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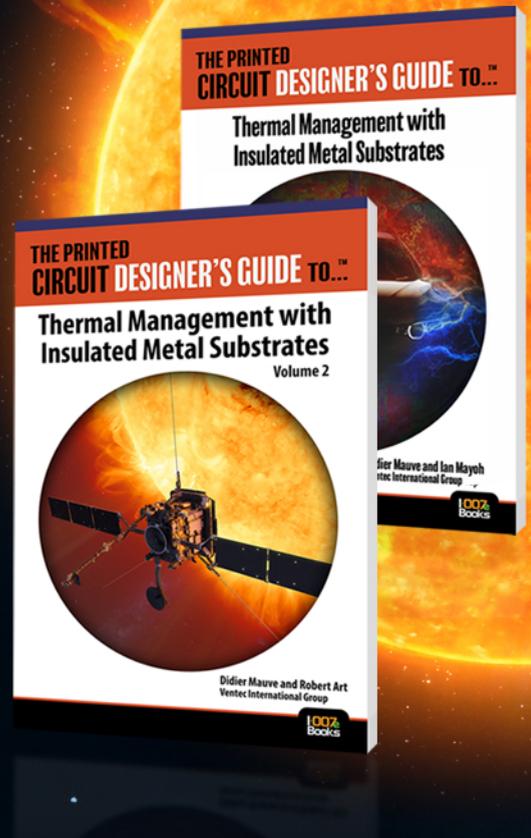
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Top Design Challenges

In this issue, we share the top PCB design challenges from a variety of viewpoints—PCB designers, fabricators and assembly providers. The three challenges most often cited by contributors revolve around DFM, communication, and data—all of which are interrelated. We think you'll find this compilation of design challenges useful.

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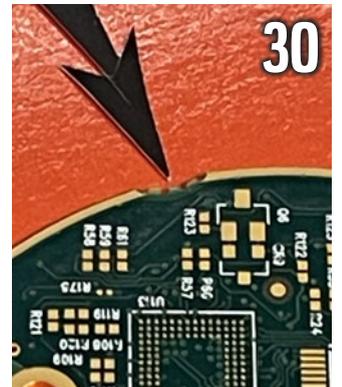
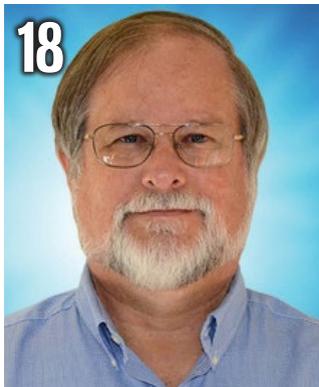
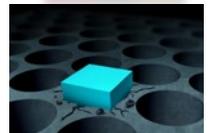
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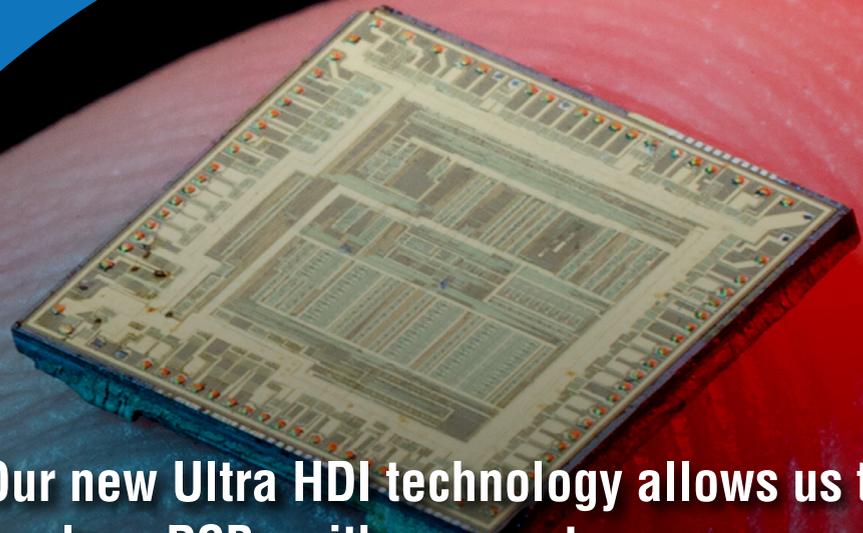
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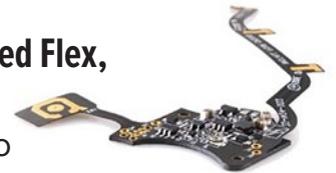
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Slow And Steady Wins the Race

The Shaughnessy Report

by Andy Shaughnessy, I-CONNECT007

You're probably wondering: Why is there a tortoise on the cover of *Design007 Magazine* this month?

In one of the most popular Aesop's Fables, "The Tortoise and the Hare," the slow and steady reptile beat his much faster opponent by taking his time and persevering. Judging from what our expert contributors have to say in this issue, many PCB design problems could be precluded if designers simply took their time. (Yes, designers even called themselves out for this.)

We asked PCB designers, fabricators, and assembly providers to share their thoughts on the biggest PCB design challenges. The three challenges most often cited by contributors revolve around DFM, communication, and data—all of which are interrelated.

DFM continues to be one of the prickliest predicaments perplexing today's designers. It's the little things—not signal integrity or EMI—that often cause the CAM department to put a hold on most designs. Several contributors from the manufacturing side address the need



for designers to visit board shops and assembly providers—and visit them often. When was the last time you toured a board shop?

On a related topic, communication got plenty of shout-outs this month, with fabricators pointing the fickle finger of fate at designers for not working with board shops until it's too late. But the reverse also holds true: Designers noted that many (not all) fabricators are reluctant to share their most up-to-date manufacturing capabilities, and that fabricators' websites often don't have the info a designer needs for a complex design.

Data was also mentioned by designers, fabricators, and assembly providers alike this month. Many pointed to the need to move on from Gerber and embrace Smart data transfer formats such as ODB++ or IPC-2581. Not surprisingly, some EMS folks stressed the need for more designers to become familiar with the CFX manufacturing format, which is now interfaced with IPC-2581 in the IPC-2591 format.

In this issue, we share the top PCB design challenges from a variety of viewpoints—PCB designers, fabricators, and assembly providers. Weighing in, alphabetically, are Dan Beeker, Charlie Capers, Kelly Dack, Michael Ford, David Hoover, Jen Kolar, Dana Korf, Scott Miller, Barry Olney, Gerry Partida, Qandeel Sheikh, Matt Stevenson, Mark Thompson, and Mark Wolfe. We also bring you articles by Frank Xu, Mark Gallant, and Mike Morando, as well as columns from John Coonrod and Joe Fjelstad.

We think you'll find this compilation of design challenges useful. Remember: Slow and steady wins the race. **DESIGN007**



Andy Shaughnessy is managing editor of *Design007 Magazine*. He has been covering PCB design for 23 years. To read past columns, [click here](#).

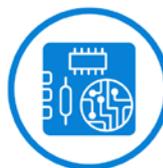


What Does a PCB Designer Do?

A printed circuit board design engineer oversees the creation of printed circuit boards (PCBs) used in phones, computers, and most other electronic devices. As a PCB designer, your responsibilities include designing the layout of the unit to incorporate the appropriate components, making recommendations to improve existing designs, and overseeing the actual manufacturing of these products to ensure they meet industry and company standards. These boards are the backbone of modern-day electronics, acting as the central unit of anything that runs on a microchip or CPU. You must design the board in such a way that it meets the specific needs of each product.

PCB design engineers must design and implement various circuit boards and perform revisions to apply changes that are based on the specifications of customers and engineers. They need to collaborate with the companies that fabricate and assemble PCBs to discuss the quality, cost-effective, and timely deliveries of PCBs. PCB designers must also use AutoCAD software to design schematics for the PCB systems.

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DESIGN CHALLENGES: From the Designer's Viewpoint



Feature Q&A by Andy Shaughnessy

I-CONNECT007

It seems like everyone has something to say about PCB designers and the way they do their jobs. Everyone involved in the process likes to chime in with advice for the front-end folks. But what do designers think about their segment of the industry? This month, we asked PCB designers and design engineers to discuss their biggest pain points.

Jen Kolar

Monsoon Solutions

What is your main concern for PCB designers?

Communication. It all comes down to that. Are they asking clear questions of their customer or manufacturer? Are they reading the customer's full email or documentation and responding to everything? Vice versa for the customer. Is someone sending key summaries from verbal conversations to make sure everyone is on the same page? How much design is happening in chat applications (Slack, Chime, Teams, etc.) vs. a more structured, traceable way? Is the customer providing the necessary data in an organized fashion or in dribs and drabs? While PCB design engineers may be good at design, they also need to be good at customer and project management. This is especially true in a service bureau environment like ours with external customers, but it still applies to internal customers.

Make sure the requirements and decisions are clear from both ends. The difference between



Jen Kolar

having a brick vs. a useful board can come down to one conversation. I see many projects drag on due to the customer being slow to reply and the designer not managing their customer well to keep them moving. Sometimes there is nothing the designer can do but, often, setting clear expectations about the inputs needed and clearly calling out when the project is on hold is a good way to keep the customer moving. The designer sometimes needs to help them realize when they aren't quite ready to move forward and that they need time to figure things out.

Designers need to be good at communicating. Depending on the scope and size of the project, daily updates of progress may be important. For much longer projects, it might



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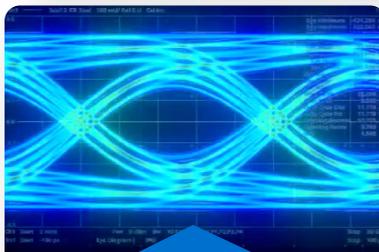
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be weekly, but the customer should not be left guessing where things are, and the designer shouldn't get too far ahead of customer review.

What issue do you think PCB designers should be more aware of?

The ever-changing technology of the end manufacturers, especially of fabricators. It is easy for designers to get caught up on “standard best practices” or “rules of thumb.” It is also common for designers to not always know the capabilities of who will be doing the manufacturing, so they necessarily (or hopefully) are more conservative in their layouts. Fabrication tolerances and practices don't always just get tighter and more advanced. The back and forth I've seen on stacked and staggered vias is one example. Thoughts continue to change on reliability of stacked microvias and each vendor or manufacturing expert will have a different opinion.

I think PCB designers should be diligent in pushing to get up-to-date manufacturing capabilities from the planned end-fabricator for each project. It may be them, a project manager, or the customer requesting the information, but taking the time, especially for more complex projects, is critical. Nothing is worse than finding out in DFM, after a six-month layout effort, that you need to increase your annular ring size or trace spacing in a dense high-speed design. The information listed on vendor websites or capabilities documents is often not sufficient to make design decisions on multilamination cycle and high-density boards. It is important to have that conversation early and not make assumptions.

What problem should PCB designers be more aware of?

Not consciously identifying the key limiting factors for a design before diving into placement or routing. Design is a balance of many requirements, often competing ones. Taking the time to be intentional and to really think

through all the factors that will govern a design is key. For example, power and signal integrity or RF requirements often conflict and tradeoffs need to be decided. Designers all too often incorrectly assume what the priority might be or, even more often, only hear partial feedback from the constituents rather than gathering all the requirements and ensuring the customer internally works through prioritization. Fabrication requirements and electrical design specifications may be very different.

Yet these competing requirements may all govern the same signals or, even more typically, the same signals may cross through regions of the board with different requirements. How you make decisions when planning your placement and routing, especially on dense, high speed, or highly constrained boards, will make all the difference in how challenging it is to route and how well it will function. Pesky late-breaking mechanical requirements, such as a mounting hole in the middle of where you placed your ASIC or keep-outs you didn't know were needed, can be devastating near the end of the design process. Layout kickoff checklists can be a great way to make sure you don't miss important questions that will drive your design. Ironically, this too comes back to good communication.

Cherie Litson

Litson1 Consulting

What is your main concern for PCB designers?

In a word: DFX. Actually, that's an acronym with a lot of baggage. But it's true that every tradeoff a designer makes, every decision a design team makes, changes the efficiency of the production and workability of the product.

What issue should PCB designers be more aware of?

Power and GND returns. These are the main sources of a noisy circuit. Placing components



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Cherie Litson

near the wrong power and ground return areas or crossing between different reference returns will create issues. The nice thing about this is you don't have to do a lot of calculations to get this right. Just be aware of where you're placing these power rails and your ground return will get you 90% there. Then adjust for specifics. Also, don't forget to check the 3D effects of your ground connections to planes for all through-hole pins to be soldered. These become heat sinks very quickly.

What problem should PCB designers be more aware of?

Manufacturing effects due to design layout. This goes back to some of the DFX issues.

During fabrication: Nothing will bump up the cost of your board faster than having a poor layer stackup. Uneven layer structures and sequential laminations are your biggest hits.

During assembly: Cold solder joints will require rework; solder mask defined pads create solder starving; unplugged vias in pads create all kinds of issues; placing components too close or sharing pin pads (besides being a J-STD-001 violation) will create a poor sol-

der joint, cracked components (large ceramic caps), and inability to rework the product if there's a bad part.

On top of it all, documentation that works. The less communication you have to individually attend to the better. The buttons in your software don't work unless you set them up properly. Know how to communicate with your manufacturers. What information do they need to make their job easier. They will reward you for that.

Dan Beeker

NXP Semiconductor

What is your main concern for PCB designers?

The focus must be on the dielectric, and the impact of the transmission line on the movement of the energy. A few critical pieces of information are needed to ensure success. You must know the switching speed of the driver. That frequency, and the resulting wavefront, tell you what you need to know about the requirements for the PCB design. Based on this data point, you know what impedance will be required for the output transmission line (do I need to control it?) and where to put the first capacitor that supplies the driver. After that, you need to know how much energy the device requires to function, which tells you what the impedance of the PDN must be. If you design your PCB based on these facts, your chances of success increase significantly.

Key Facts

- Electromagnetic fields travel in the space between the conductors, not in the conductors.
- All energy is moved by wave action.
- The transistors' switching speed determines the operation frequency, not the clock rate.
- Signal and power connections must be one dielectric from ground for their entire length (including layer transitions).



Dan Beeker

What issue should PCB designers be more aware of?

It is simply the need to understand basic science. This should drive the underlying philosophy for the board design. The focus must be on designing the spaces where the energy is moving. The copper structures, foil layers, and vias are used to define the spaces, or more properly, the waveguides on the PCB. The two-dimensional approach that is most commonly used must be redefined into a three-dimensional structure. Each signal or power conductor is only one part of a three-piece structure. The three elements needed to control the field must be present to achieve good signal integrity and EMC.

The Rules of Triplets

- You only need three components to use to contain EM energy: Conductor, spaces (dielectric), conductors.
- You only get three components to use to build electronic systems: Conductors, spaces (dielectric), switches.
- You can only do three things with electromagnetic field energy: Store it, move it, or convert it to kinetic energy.



sustainability in logistics



The most obvious area of concern for logistics sustainability is the reduction of the carbon footprint. But Christian Wendt, marketing and communications department head at Siemens Digital Logistics, suggests that there is much more than simply fossil fuel costs. Wendt explains a wide variety of logistics-related areas to consider in this edition of *On the Line with...* brought to you by I-Connect007.



LISTEN NOW

Remember: We are all just plumbers using very leaky water pipes. We design three-dimensional spaces for managing EM field movement. This is not rocket science.

What problem should PCB designers be more aware of?

Engineering teams worldwide face increasingly difficult challenges in designing electronic products and achieving good signal integrity and compliance. The status quo had become to expect the design to fail EMC testing, and not just once, but three, four, maybe even five times. Each time the design is sent to be retested, there is little confidence in success. This cycle is expensive in both the time it takes to redesign the product and the cost of expediting fabricating the new PCB and assembly. Add this to the cost of retesting the product, and the numbers add up very quickly.

This expense and delay in product certification are not in the budget or the schedule. The expense not only directly affects the bottom line of the electronics supply company, but also affects the customers waiting for the product. Instead of designing the next big thing, teams are trying to fix the current one. Billions of dollars are lost each year designing products that most likely will not work. The key here is to remember that we all are involved with developing products that generate, control, and consume electromagnetic field energy. Following the rules for managing this energy will result in success.

Scott Miller

Freedom CAD Services

What are the problems, concerns, or issues that PCB layout designers should be more aware of?

The answers can vary widely depending upon the perspective of the person answering. It's assumed that the layout designer should have a strong command of the software and its



Scott Miller

capabilities, and the questions are more aimed at technical aspects that can make or break a design.

If you ask a design engineer, you are likely to hear items such as:

- PCB designers need to be very detail oriented. Pay close attention to the schematics. Designers should be aware of the small details that can often get missed. It's a good practice to have a checklist to ensure that you're consistently covering all the bases.
- Placement is the one of the most important steps in the PCB design process. Special care needs to be expended at the placement stage to save time and effort on the rest of the design.
- Pull the datasheets of the key components and follow their recommendations when you can, especially for placement. Guessing where to place parts can impact the design's integrity.
- Creating a PCB layout requires the PCB designer to be very detailed oriented. Designers should be more aware of the small details that often get missed. As a designer, you should have your own checklist. If you design a board and there is a problem, the

designer should fix it, and then document it. On the next design, go through your list before you release it for any other types of review.

- Vias need to be dropped in an organized fashion, on a grid system, during the placement stage for designs with a lot of connections. Vias placed in a random fashion cause headaches during the routing stage and can choke off the power planes.

If you ask a manufacturer, you may hear:

- Manufacturability matters, and it matters much more than just meeting minimum requirements. Optimization for manufacturing process tolerances is critical for acceptable yields in a high-volume environment. Understanding manufacturing processes that allow the designer to consider tradeoffs to create this optimization is important. For example, some rules are for initial manufacturing, and some are for rework. Initial manufacturing takes priority.
- By being aware of manufacturing capabilities, tolerances, and constraints during the design process, designers can create PCBs that are more efficient and cost-effective to produce. A focus on DFM helps to reduce the number of manufacturing errors and rework, shorten production times, and lower overall production costs. Designers must consider various aspects, such as appropriate trace widths, via sizes, and component clearances, along with the selection of suitable materials and surface finishes.
- Clean, correct, complete data is important. Relying on fab shops to make edits to meet requirements creates a disconnect between the design database and the actual product. If these updates aren't captured in the design database, future respins will require edits to be made again, and it is unlikely those edits will be the same. With a respin, it is a common misconception that, "We built it this way before so it's good." What was built is what the fab shop edited.

- There is a difference between drill size and finished size and how that impacts the use of press fit connectors. There are risks associated with allowing the PCB manufacturer to determine drill size. These should be determined on the design drawings.
- Know the design requirements such as export restrictions, ITAR, EAR, ESD/SMI, safety, environmental, Class 2, Class 3, and space specifications. All these need to be identified and their implications understood up front to ensure they can be met during the design process.

If you ask a signal integrity engineer, these will probably be at the top of the list:

- Signal integrity needs to be a priority, particularly in high-speed designs. It is one of the most critical factors that PCB designers should be aware of. Maintaining signal integrity ensures the reliable performance of a PCB, and designers need to be aware of aspects such as impedance control, crosstalk, and reflections, which can impact the quality of the signal.
- They must employ proper routing techniques and carefully consider component placement to minimize the negative effects of these factors. Additionally, the use of termination resistors can help maintain signal integrity and prevent signal degradation.
- Selection of a stackup, appropriate materials, routing plans, and the use of power planes as a reference can all impact the performance of high-speed signals.
- Be sure to recognize the importance of ground return vias for transitioning between layers. Insufficient vias will impact the performance.

So, it's important to understand that the answer you get will depend upon who you ask and their place in the design and manufacturing cycle. Whoever you ask will be sure to have a unique perspective. **DESIGN007**

DESIGN CHALLENGES: From the Fabricator's Viewpoint



Feature Q&A by Andy Shaughnessy
I-CONNECT007

If you're a fabricator, chances are you have a few things to say about at least a few of the PCB designs that make their way through your shop. I guarantee that you have several well-worn stories about designs that made you scratch your head and think, "Hmmm."

So, in this section, we asked PCB fabrication experts to share their thoughts about challenges that PCB designers need to more thoroughly understand. Do you see yourself on either side of these issues?

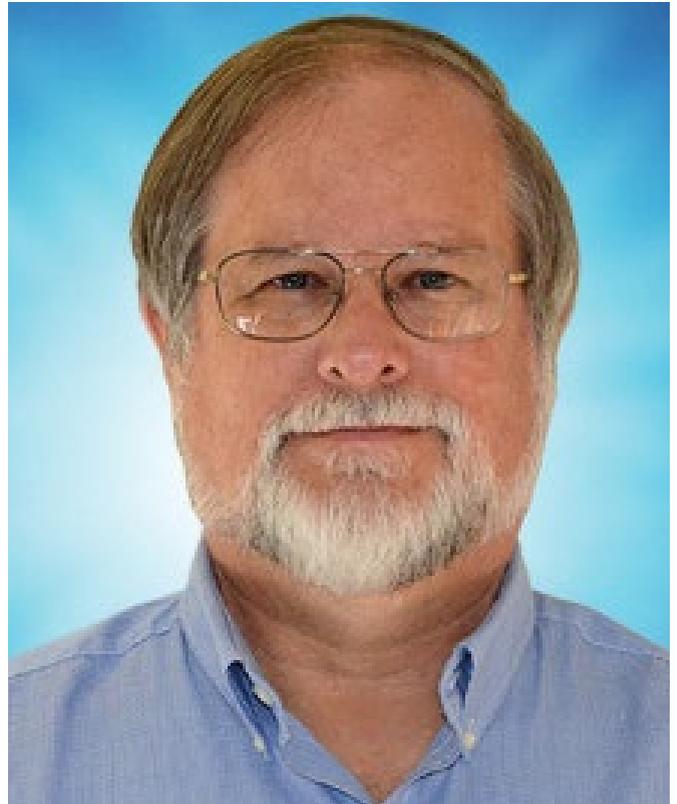
Dana Korf

Korf Consultancy LLC

What is your main concern for PCB designers?

Impedance and signal loss variability. In recent years the signal integrity that RF designers were very concerned about is now becoming a requirement in standard digital and analog designs. Simulation tools are used to characterize the design nominally and against high and low tolerances of the key specifications. Then a quick prototype is fabricated and tested. Several iterations may be built and assembled until the proper answer is achieved.

The signal performance can be affected by the drilled/lased hole's inner diameter, plated diameter, material dielectric thickness and electrical properties, solder mask, Dk and thickness, trace-width tolerance, and to a



Dana Korf

lesser extent its thickness. Yet, the fabricator is rarely required to provide this information to the designer. So, the designer doesn't know if the PCB was built at the high-end, low-end, or middle of the tolerance range. Designers often complain that a new revision or build didn't perform like the last version. Of course, it may not. The reason is most likely due to fabrication tolerances.

When the design has tight impedance or loss requirements the designer should require more information about the received PCB crit-



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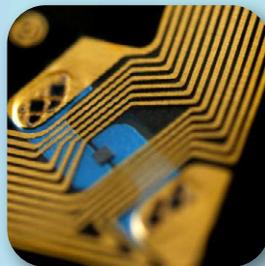
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ical parameters to better correlate actual performance to the expected performance.

What issue should PCB designers be more aware of?

Over-specification. Significant cost is incurred by overspecifying requirements. One of the most common reasons for this is that requirements get copied from one design to another design without the designer's full understanding of whether they are applicable. Another reason is that PCB hardware engineers and designers are not sufficiently taught about cost impacts early in their career. For instance, how many PCB fabrication classes are taught at trade schools, community colleges, and four-year universities?

Every day I listen to my Apple iPod that is 20 years old. It is a consumer product and probably wasn't designed or expected to last this long. I wonder how much cost was specified into the PCB that wasn't required for a board that only needed to last five or so years? How much revenue has been lost because I haven't needed to replace it?

One common example of over-specification is the lack of use of IPC Class 1 requirements. These were intended to provide sufficient margin for the system to operate with a short lifetime. But most non-Class 3 designers specify the PCB to be Class 2 by default. Decreasing the Class from 2 to 1 has the potential to increase the production yield, reduce processing cost, and reduce material cost, thus reducing the product cost.

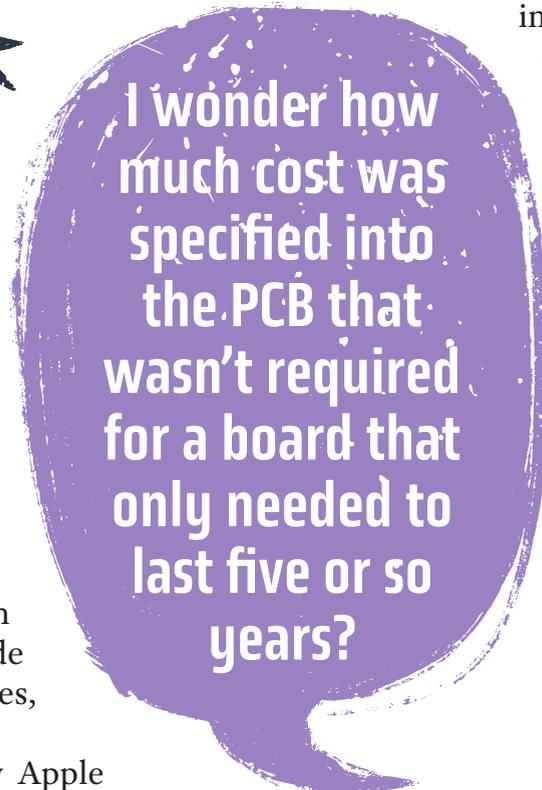
What problem should PCB designers be more aware of?

Documentation package quality. Designers who send their data to fabricators and assemblers with Gerber-based packages require the manufacturer to manually interpret the drawings and specifications and manually associate and enter the requirements into their CAM systems. For example, a separate netlist is required because it is assumed that the data may be wrong. Trace thickness is also manually entered.

The industry has had intelligent data formats available for approximately 25 years. The formats are the Siemens ODB++ and IPC-2581 formats. It has been shown that less than 25% of all data packages are based on these formats.

These are intelligent data formats that transfer the intelligent data from the CAD systems to the CAM systems such that they can automatically load a significant amount of the data without human intervention. These intelligent formats also don't require as many ePaper documents, such as a fabrication drawing, bill of materials spreadsheet, stackup drawing, etc. There are often discrepancies between supplied documentation duplicate information that is sent. This extends the production or prototype cycle time and introduces errors.

Designers should immediately work with their suppliers and switch to IPC-2581 or ODB++ to immediately reduce their design cycle time and improve data transfer quality.



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Dave Hoover

TTM

What is your top concern for PCB designers?

Today's PCB designers need to have better awareness of actual manufacturing tolerances and capabilities. They need to work with their fabricator's application engineer to fully understand the board shop's capabilities.

What issue should PCB designers be more aware of?

When selecting a material, designers should pay attention to the support and services provided by their material supplier. Remember: It's not all about price.

What problem should PCB designers be more aware of?

Designers need to know the difference between short-run NPI (QTA) vs. mass production quantities. There can be vast variations between the two; it's easy to hold a tighter tolerance on QTA lot sizes.



Dave Hoover



Gerry Partida

Gerry Partida

Summit Interconnect

What is your main concern for PCB designers?

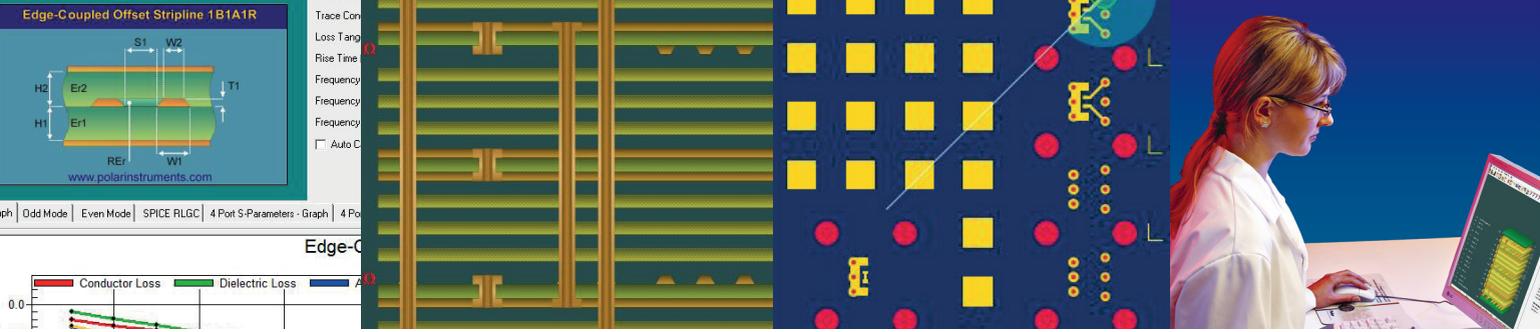
More designers must pay attention to the minimum conductor thickness on internal buried/blind layers.

What issue should PCB designers be more aware of?

Calculation of a pad size to Class 2 or 3.

What problems should PCB designers be more aware of?

Non-functional pads and drill-to-copper distance; there is no extra routing space. DESIGN007

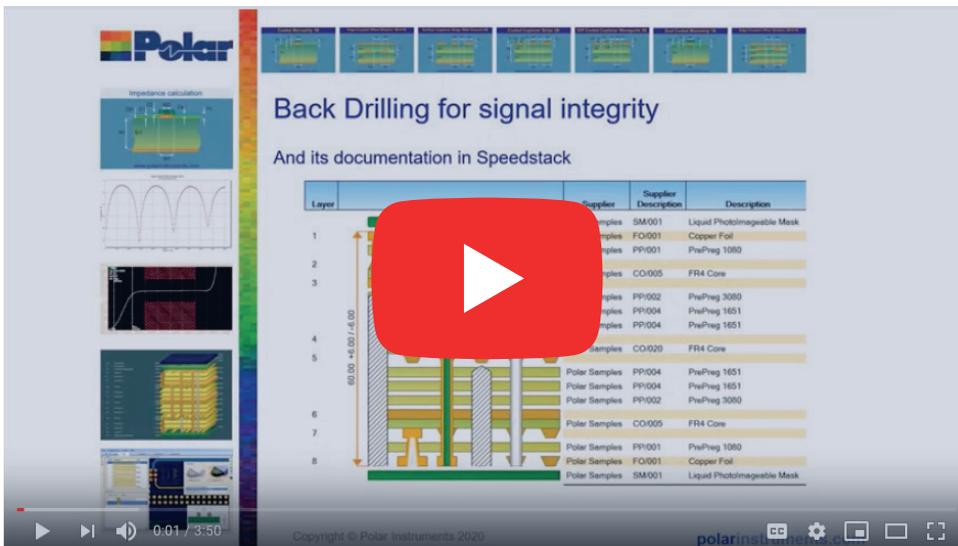


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DESIGN CHALLENGES: From the Assembler's Viewpoint



Feature Q&A by Andy Shaughnessy

I-CONNECT007

Fabricators are fairly vocal about the design issues that they encounter, especially with brand-new customers. They are, after all, the next step in the process. But we don't hear as much about design issues from EMS providers.

This month, we asked experts from the PCB assembly segment to share their thoughts about design challenges that affect technologists on the EMS side. They offer a look at the world of PCB design from downstream in the process, and they raise several interesting points.

Have your assembly partners offered you any advice on design for assembly (DFA) techniques?

Michael Ford

Aegis Software

What is your main concern for PCB designers?

Design for sustainability (DFS), including the right to repair, product and material reuse, and effective recycling, as well as the CO₂ and energy impacts of materials and products are the sustainability credentials that customers across the industry are building into their requirements. The industry has a choice—to be driven by carrots from customers in a way that is good for them and the industry, or wait for the inevitable sticks from governments, which typically introduce a sudden burden without a focus on complementary benefits.

Designers need to take extreme care now when defining and measuring their designs against these emerging requirements. They



Michael Ford

must understand how to benefit from these requirements and be able to communicate information in a way that ensures the privacy of IP. Emerging technologies address these concerns, but to save investment and expense, they should be adopted in a way that creates interoperability throughout the industry.

Unlike manufacturing, where a single partner is responsible for producing many of the same product line together, the recycling of products happens at random as individual products reach end of life. Information for sustainability must therefore be available more widely, smartly, and more securely. A holistic discussion is needed.

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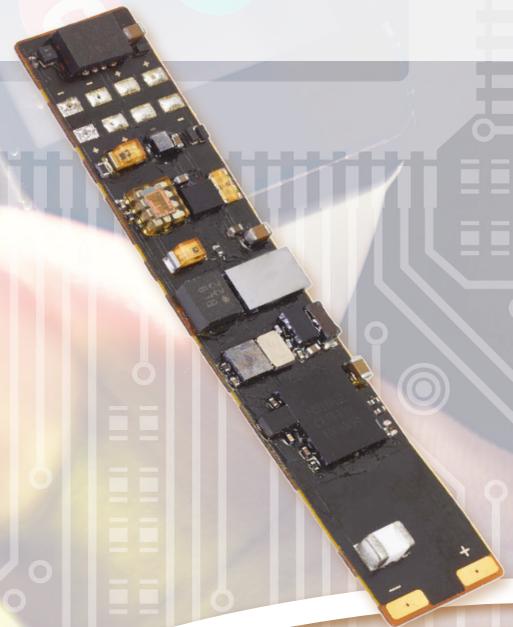
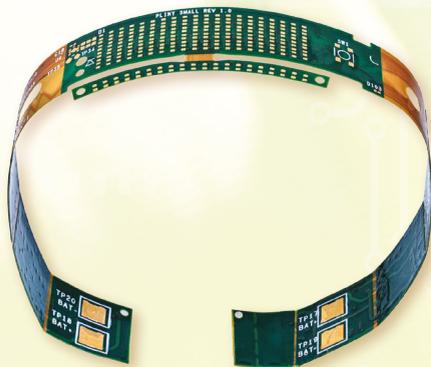
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What issue should PCB designers be more aware of?

Designers continuously learn how to improve their designs. A significant contribution to this process is information related to manufacturing, actual materials used, and the way that the product is used in the market. The issue here is that context is very important. Results of customer feedback, warranty claims, and reliability of the product in the market are affected by several variables which design does not currently have visibility of nor control over.

The same product may be manufactured at several different locations, with different configurations and settings, all of which alter the manufacturing performance. The choice of materials often deviates from expectations, as material shortages or increased costs trigger the use of local or more cost-effective materials. These may perform differently in certain conditions. Customers may use, and abuse, products in certain applications. How can all these factors be measured? Understanding the results of product design decisions means that detailed context of manufacturing, materials, and use-case information is essential if we are to create better designs that reduce the cost of manufacturing, poor quality, and exceptions occurring in the market. The use of solutions around an interoperable digital twin architecture standard, such as IPC-2551, may be the way forward.

What problem should PCB designers be more aware of?

Designers hold a very important key, the first step in the digital transformation of manufacturing and the supply chain. Habitually pressing the “Output Gerber” button in design tools is crippling the Smart manufacturing effort. The problem is that designers are uncomfortable in considering potential inefficiencies and security risks in their current way of operation. Designers must be aware that modern, Smart product data formats, such as IPC-2581,

in the hands of the right manufacturing engineering tools, eliminate the need for manual data manipulation. This inevitably causes long lead-times, wasted costs, and risk of mistakes, all of which are common with a Gerber-centric output. A single file format, such as IPC-2581, can be more easily secured, need not be opened or seen by a human, and contains only the necessary data needed to manufacture the product.

Going forward, with the utilization of another IPC standard, IPC-2591 CFX, solutions can be possible that allow manufacturing of products without the disclosure of the design data in any holistic form. The problem is that, statistically, design management has their heads in the sand when it comes to Smart data flows that are essential for the success of digital manufacturing.

Qandeel Sheikh

Whizz Systems

What is your main concern for PCB designers?

Understanding the purpose and application of the PCB. Designing a PCB involves more than just creating a layout. It’s essential to consider the purpose and application of the board. This includes its interfaces, technology, form factor, and electronics circuit design. When designing high-density applications with very fine-pitch components such as 0.4-mm BGAs, it is important for the designer to have a clear understanding of fan-out techniques such as stacked microvias, laser vias, skip vias, HDI, and VIPPO (vertical interconnect process with plated over) that are used to escape out and route such components on the PCB.

PCB designers should have a sufficient understanding of the electronics circuit design and schematics to ensure that the board layout aligns with its intended purpose. For instance, a PCB designed for a communication system will have different requirements than the one for a power supply system.



Qandeel Sheikh

For complex PCB technologies, designers should consider various factors that impact the cost of PCB production including material selection, copper weight, PCB size, number of layers, finish options (ENIG, HASL, etc.), and minimum trace width and spacing requirements.

What issues should PCB designers be more aware of?

Thermal management and signal/power integrity are critical concerns that require careful attention during PCB design. EMI compliance, power handling of high and low voltage, and ensuring signal integrity are all critical aspects of PCB design. For example, sometimes isolating digital and analog signals becomes challenging in a miniature form factor. The same issue can also be observed for high- and low-voltage power rails.

The transmitted data may be distorted, interfered with or attenuated, leading to an inaccurate or unreliable result. PCB designers must design the board to prevent issues such as signal reflections, crosstalk, and electromagnetic interference (EMI) by following best practices of signal integrity, proper grounding, shielding, and routing techniques.

High-powered boards with high component density and high-speed signals also present heat-related issues that require careful management. The designer needs to ensure that they strike the right balance between heat dissipation and power-related issues when increasing copper size/thickness. PCB designers need to carefully consider the placement of heat-generating components, such as processors, power chips, or high-power LEDs, and design appropriate thermal management solutions, such as heat sinks, thermal vias, and copper pours, to dissipate heat effectively and maintain optimal operating temperatures.

Are there any technologies or processes that PCB designers should be more aware of?

The manufacturing and assembly processes. PCB designers need to design with manufacturing and assembly processes in mind, especially when designing for assembly and test (DFx). This can be done by ensuring that the physical layout does not violate processing capabilities, considering how the physical layout will interact with the assembly process, and making design considerations for testing the boards. Additionally, designers must ensure that the assembled PCB does not interfere with mating PCBs and other mechanical parts. For instance, the designer must know how to design the board with sufficient tolerances and clearances for proper installation of heatsinks and enclosures.

In a nutshell, designing a PCB requires a comprehensive approach that considers the board's purpose and application, thermal management, signal and power integrity, and manufacturing and assembly processes. Designers should have a clear understanding of the underlying principles and values that drive these concerns to ensure that their designs are not only technically but also functionally sound. This will promote accuracy, reliability, sustainability, efficiency, and simplicity in their designs.

Mark Wolfe

IPC Executive EMS Advisor

What is your main concern for PCB designers?

As component lead counts increase and lead spacing decreases, the potential for defects in the manufacturing process has grown as well, resulting in industrywide increases in rework and scrap costs. The most recent IPC Quality Survey showed that the costs of rework and repair have grown by 2x or more over the past four years. At a minimum, rework costs for many newer components require more expensive equipment and/or more time-consuming processes. In a growing number of products, full PCBAs may need to be scrapped as some of these complex components may have heat limitations or may be inaccessible to even allow for proper rework.

The potential for difficult or impossible rework that can result from tight package-to-package spacing or package heights can often be avoided with the proper emphasis during PCB design. Rework and scrap concerns have not been a historic point of emphasis for PCB designers, at least not until fairly recently. Regardless, the PCB design community can play a significant role in mitigating these growing costs by putting a much greater focus on design for rework and scrap as they make PCB design and layout tradeoffs in the future.

What issue do you think PCB designers should be more aware of?

As the electronics manufacturing world has experienced some of the painful implications of lean, but ultimately fragile, supply chains over the past few years, there has been greater emphasis placed on multi-sourcing of key components. Raw PCBs generally fall into this category and companies that are trying to be more agile in dealing with disruptions are thinking differently about their PCB sourcing.



Mark Wolfe

The more that PCB designers can proactively keep options open without sacrificing design parameters or creating undue risk, the better. Try to specify and test multiple materials that meet your requirements whenever you can. You should design panels that are reasonably optimized for multiple PCB suppliers as well and avoid tuning yourself to a single source. It won't be commercially viable in all cases, but having the option will be beneficial.

What problem should PCB designers be more aware of?

Virtually any PCB design tool today will generate a data file for stencil generation, subject to default rules and/or whatever rules the PCB designers may implement. In most cases, those files are directly transmitted to the stencil supplier.

Unfortunately, the loop is not necessarily fully closed back to PCB design when issues are found on the manufacturing floor. It is not unusual for the stencil supplier to receive a set of additional adjustments from manufacturing that modifies various types of apertures to address their issues. Over time, those become standard adjustments as the stencil supplier translates the data file that they receive from PCB design into what they believe manufacturing wants.

Ultimately, it is never a good practice to have such differences between the intentions of design tools and the actual process execution. While the manufacturing floor would ideally provide feedback to PCB designers when they make changes at the stencil supplier, this is not a given. Make sure your PCB designers reach out to their stencil house and their manufacturing floor to help keep the right feedback loop in place.

Charles Capers

Zentech Dallas

What is your main concern for PCB designers?

Designers need to be more focused on the processes that take place after the design is complete, namely, PCB fabrication and assembly. Most designers have never stepped foot into the fab shop or EMS facility that will be completing the manufacturing of the product. It is critical to understand the processes that go into building their design, and how difficult it can be to build a poorly designed product. Visit a variety of fabricators and assembly providers; they'll be glad to answer any of your questions, and you might learn a few things in the process. Remember, your PCB design is not the final product.

What issue should PCB designers be more aware of?



Charles Capers

Designers need to pay more attention to design for manufacturability (DFM), design for assembly (DFA), and design for test (DFT). IPC standards are a great way to learn the do's and don'ts of product design and manufacturing. I am a big fan of the CID/CID+ certification curriculum.

What problem should PCB designers be more aware of?

PCB designers should be more aware of the operating environment of their designs. Where is your board going to be during its lifetime, and in what type of environment? It is important to know how extreme temperatures, humidity, vibration, and other environmental factors can have a huge impact on product failure in the field. **DESIGN007**

Keeping Your Design on the Road

Target Condition

Feature Column by Kelly Dack, CIT, CID+

Is CAD data output enough to move your design through to global manufacturing success? Form, fit, and function are often referred to in the context of part interchangeability. How well will parts fit together with other parts after rolling off a manufacturing production line? Without key specification limits for these physical performance requirements, a PCB design is destined for quotation delays, no-bids, or outright manufacturing rejection. These can kill time-to-market product development goals.

CAD Data is Absolute

If you have ever opened a CAM file generated from your CAD layout tool, you have seen hundreds of numeric values, each representing a geometric data point in the design. Some of these values specify where the center of a trace is to be located after printing, plating, and

etching. Some values represent a location for the center of a hole to be drilled or a milling path for a slot or board edge. Some of the data tells a machine how fast to spin and where to rotate or move to perform the work. All CAD layout tools output absolute data, and those points nominally represent the exact, theoretical position—the target condition—of a geometric feature.

CAD Data Doesn't Account for Manufacturing Process Tolerance

Manufacturing tools, machinery, and materials introduce a vast, complex set of subjective variables for which the manufacturer must adjust to match the manufactured part feature to the absolute dimensional design data points. But since perfection in manufacturing is nearly impossible to achieve, the challenge for the manufacturer is to know how far a processed

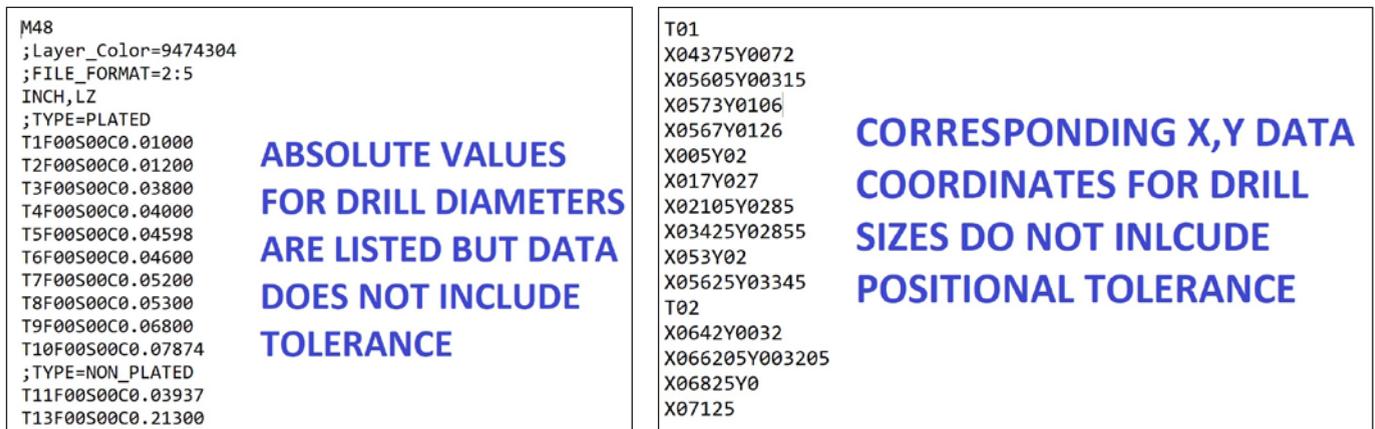


Figure 1: Two drill data files.

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feature can stray from perfection and still be form, fit, and functionally acceptable. For example, in a PCB outline, the absolute CAD data may reflect a horizontal (X direction) value of 6.00937". But there is not a machine, material, or process in our universe which can form a glass-epoxy laminate board to such a degree of accuracy. When a PCB designer's data shows a coordinate of 6.00937" and a run of parts are cut measuring 6.006", 6.012", 6.013" and 6.014", must they all be scrapped? Who says, and by what criteria? Manufacturing stakeholders must be given a range of dimensional acceptability because the yield of their processes vary.

Setting Your DRC Within Legal Limits

Drive down a country road and you're bound to see a speed limit sign. How do you process this and adjust your driving speed? Whatever your process, you are considering a driving constraint and making the first attempt to hit the target condition for a rate of speed. If the posted limit is 60 mph, most drivers will adjust

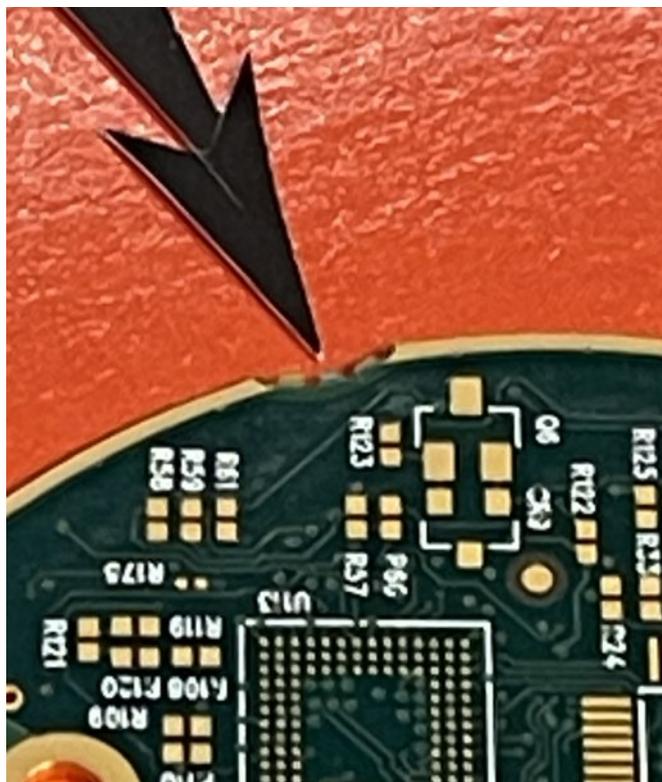


Figure 2: Board edge mouse bite.

their car's rate of speed right up to the limit. Why? Is it human nature to set things right to the edge? Do we think—erroneously—that by setting a complex system to a particular value the result will be exactly 60 mph? It will not. "Exact" is subjective to the context within which the subject must inter-relate with other parts of the system. This is especially true when it comes to the complex systems applied in volume production.

The manufacturing system which produced the car's speedometer and cruise control module is subject to a "stackup" of manufacturing process tolerances. As the modules are assembled, they must be calibrated for accuracy due to the differing manufacturing variations. To compound the challenge of system accuracy, these modules are then installed into automobile systems which have another set of system variables the manufacturer cannot foresee. The variables of heavy, off-road tire diameter, road grades, and differing temperatures will challenge a cruise control system's ability to achieve any kind of consistent perfection. According to the NPR program "Car Talk," cruise control systems can vary from the set value by a factor of $\pm 10\%$. So, even if you set the cruise control at 60 mph, the variables in play could send the car whizzing by a county sheriff at 66 mph. You may soon be having a discussion with the local gendarme about accounting for tolerance when setting the cruise control. Should we all set our cruise controls to 54.5 mph to allow for a system tolerance of $\pm 10\%$?

DRC Settings Must Allow for Manufacturing System Tolerances

Generally speaking, PCB designers manually adjust their CAD tool's DRC settings like a driver sets a car's cruise control. Many inexperienced designers set DRC values to the "reduced manufacturability" Class 3 limits supplied by local prototype suppliers. If a hot-shot prototype supplier can provide .003" finished traces and spaces, designers are somehow inclined to set the DRC for .003" traces and

spaces. If the proto shop says they can produce within an impedance tolerance of $\pm 2\%$, many times we find that same strict value stuck in the fabrication notes even though a more lenient value would perform sufficiently.

Some designers think that a proto supplier's CNC drilling equipment is so accurate that annular ring sizing can be drastically reduced without concerns for breakout conditions. They fail to understand that drilling tolerances are only part of the system PCB manufacturing operation and attributes which must come together in order to perform a concentric plated through-hole. There are also printing, etching, and plating variables. There are even material stretching, expansion and contraction factors which the supplier must allow room for. In the often-misunderstood world of PCB prototyping, an amazing feat of fabrication success is deliverable, even when the design layout is red-lining on the upper limits of prototype supplier capabilities.

But what many PCB designers do not understand is that in order to furnish the extraordinary, "impossible" design capabilities mentioned in their advertising, the proto shop will have to build ridiculous amounts of extra parts to yield enough to deliver the small order. Now, it may be easier for some to realize why they are being charged \$500 each for that quick-turn run of 10 tiny PCBs: \$4,500 of the order went to pay for time and materials for the other 100 parts on the manufacturing panel which did not meet spec and had to be scrapped. The cost was high because the yield was so low.

In fact, for a few years now, CAD tool companies have picked up on this trend and have been working with PCB manufacturing companies to capture their capabilities—their speed limits, so to speak—in hopes of PCB shops developing automated design "cruise controls" for layout in the same fashion as towns, counties and states post their speed limits.

The outcomes of these endeavors have been hopeful at best. They have been able to publish some design constraints and even automati-



cally provide a quote after running a quick, automated DFM review based upon their own unique manufacturing constraints. "Just set it and forget it" is the DRC concept being sold here. This business strategy makes a lot of sense to quick-turn prototype suppliers and CAD tool companies. They are trying to solve the problem of their tools being used to create unmanufacturable PCBs.

But guiding next-generation PCB designers to use rules uniquely achievable only by these isolated resource service arrangements seems to miss the point when a design must eventually scale to production. The real world of volume manufacturing requires more relaxed DRC settings for volume, cost constraints, and design material allowances. If our volume manufacturing stakeholders had a nickel every time they heard a customer complain, "Well, the prototype shop could do it," they could all retire. Unfortunately, by way of our onshore, custom prototyping capabilities, many PCB designers are groomed to expect their offshore stakeholders to machine to exact numeric values and meet exact material and stackup recipes.

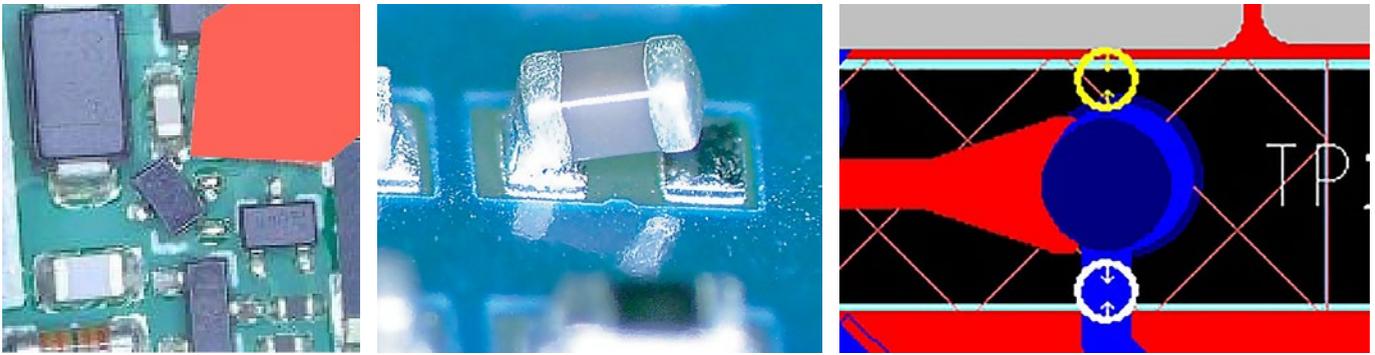


Figure 4: Three examples of data “car crashes.”

How Tolerant is Your PCB Design Layout?

Have you ever been to traffic school? Years ago, I sat in a room with other offenders listening to rules about driving that I thought I already knew. It all seemed quite boring until we got to the slideshow of actual images of accident scenes. These images depicted the potential cost of operating a vehicle system outside of the acceptable limits.

Similarly, PCB designers cause accidents caused every day by operating their layout tools on cruise control. PCB designers are being given the “keys” to PCB layout tools with default settings they do not understand, producing data output to be supplied to PCB manufacturing stakeholders whose capabilities are off their map. Fabrication and assembly stakeholders see the real-world cost of operating outside your EDA tool’s limits in the form of shorted connections, hole breakout, non-wetted leads, poor solder fillets, and tombstoned components. You can see some of these non-conforming images for yourself in the PCB acceptability standards IPC-A-600 and IPC-A-610.

The current buzz about using artificial intelligence for PCB layout could compound the issue of PCB designers not understanding global limitations, and could drive the PCB layout process autonomously. From what I gather, these visionaries do not appear to be partnering with global manufacturing supplier constraints in mind. Some are partnering with costly, smaller scale, onshore fabrication and assembly services which specialize in proto-

type quantities. We in volume production often hear from our customer’s project management team leaders who want to scale their assemblies without loosening design constraints: “Well, our proto shop never complained. Why are your suppliers seeing issues now?”

‘Traffic School’ for PCB Design Engineers

Have you ever attended a traditional drafting school? Surprisingly, it is possible to earn a four-year electronics engineering degree without ever taking a design drafting course. Our brilliant EEs, young and old, seem to know everything about “design automation,” electromagnetic fields, physics, and how to make electrons flow. But expecting them to pick up a CAD tool and create a manufacturable PCB design is like giving an inexperienced driver the keys to an autonomous vehicle not set up for busy traffic. Without any training, they are led to believe the intuitive settings will finish the job with little understanding of what’s really required behind the scenes.

A meaningful, thorough understanding of manufacturing tolerance specification is required to create a successful PCB design. A PCB is a component which must perform by interfacing with hundreds or thousands of other mechanical component part features, all while supporting the electrical requirements of the design. Remember, nothing is perfect; everything has a tolerance. It is the job of the PCB designer to consider cost and performance constraints from all the project stakeholders for the design to achieve success. Yes,

QUESTION	Questions	FACTORY RECOMMENDATION	FIG	CUSTOMER REMARKS
1	The line width tolerance is +/-20% per IPC class 2 standard, ±10% is tight for us to control.	Propose to relax to +/-20%.	fig1	Customer Response Required
2	It required solder mask for both sides, but there is only one solder mask layer in gerber.	We will print solder mask on the whole bottom side.	fig2	Customer Response Required

QUESTION	Questions	FACTORY RECOMMENDATION	FIG	CUSTOMER REMARKS
3	The final PCB thickness excludes solder resist per the stackup detail, but the whole bottom side is covered by solder mask ink.	Propose to control the final PCB thickness include copper and solder resist.	fig3	Customer Response Required
4	The final PCB thickness tolerance 62mil±5% is too strict for us to control because the core tolerance from our supplier is +/-5mil.	Propose to control as 62mil+/-10%(include copper and solder resist).	fig3	Customer Response Required

QUESTION	Questions	FACTORY RECOMMENDATION	FIG	CUSTOMER REMARKS
5	We are not sure the black solder mask is matte or glossy.	Glossy Black.	fig4	Matte Black Preferred
6	The surface treatment is not clear.	Propose to follow LF HASL.	fig5	ENIG Preferred

QUESTION	Questions	FACTORY RECOMMENDATION	FIG	CUSTOMER REMARKS
9	The outline of unit in panel is mismatch with the gerber.	Follow "gm4" layer in gerber to build the unit outline.	fig8	Customer Response Required
10	The right corners can't be built by routing .	Propose to change the inside corner to R0.5mm.	fig9	Customer Response Required

QUESTION	Questions	FACTORY RECOMMENDATION	FIG	CUSTOMER REMARKS
11	Some Φ15mil holes are partly overlapped with the solder mask openings on top side, which will lead the solder mask ink encroach on pads.	Propose to shave opening 5mil bigger than holes per side and plug these holes with solder mask ink.	fig10	Customer Response Required
12	The spacing between pads is only 12mil, and there is silkscreen line between pads. But we need at least 16mil spacing.	To avoid silkscreen onto pads, propose to delete the silkscreen lines between pads when the spacing less than 16mil.	fig11	OK

QUESTION	Questions	FACTORY RECOMMENDATION	FIG	CUSTOMER REMARKS
13	The marked dimensions in inches in the drawing are rounded off and there is deviation.	Follow gerber to do and control these data in millimeter.	fig12	OK

Customer Signature: _____

Figure 5: DFM “speeding tickets”.

we have “intelligent data,” and we are moving toward data for Smart manufacturing. But CAD data output is still absolute and the systems which presently create PCBs are subject to variables which affect performance. The question remains: By how much can performance vary? Limits of variation or tolerance must be calculated and declared if a PCB is going to work within a system.

It is not until we get outside of the data onto the PCB fabrication drawing that we hope to see the acceptance criteria for the feature. When quality assurance inspectors can see a dimension and tolerance callout specified for the edge-to-edge distance on the PCB outline, they know the acceptance criteria. They know the range of allowable form. If the designer has calculated the dimensional range correctly,

the part is guaranteed to fit and function with other mating parts in the next assembly.

PCB fabrication and assembly drawings are still the common means to communicate tolerances. There has been much headway in documentation automation. But with next-generation PCB designers entering the industry without training, we are now seeing automatically output PCB drawings missing the very specifications that they are intended to convey.

Long ago, PCB designers learned the foundational aspects of the trade as a branch of a more in-depth design drafting program offered by community colleges. These programs helped teach the language of engineering: documentation concepts (including geometric construction), third-angle projection, ANSI standard drawing practices, and the fundamental aspects of geometric dimensioning and tolerancing (GDT), to name just a few. With very few of these school programs available to teach the documentation process, manufacturing engineers are often left scratching their heads while trying to quote or produce a PCB. CAD tool suppliers have done only half the job by evolving capabilities to perform drafting and documentation.

As in all things, capability without understanding can be as dangerous. The industry continues to see an onslaught of documentation output by new designers who are “running with scissors.” Now, with auto-dimensioning capability, we are seeing dozens of unnecessary dimensions added to parts inappropriately, causing double-dimensioning nightmares. We see auto-generated PCB stackup details embellished with laminate attributes which were clearly not understood by the designer and cannot be produced. Who will finish educating our designers on how to wield these tools?

Global Autonomous Design and Manufacturing Still a Distant Vision

In driving school, we learned that the prima facie speed limit means, “Do not drive faster or

slower than conditions permit.” Always safely adjust for the surrounding conditions. Anyone who designs a PCB must be in touch with the prima facie limits of manufacturing specification and tolerance capability. Our industry continues to preach this prima facie concept through DFM. But this concept has become so subjective it is rendered meaningless to our global manufacturers. How can designers incorporate DFM if they don’t know the production supplier or manufacturing capabilities? PCB designers are the last to know where in the world their design may be produced as it scales to volume.

Free DFM reviews by onshore prototyping services read much differently than DFM reviews from China, Ireland, India, or Vietnam. Adjusting a CAD tool’s DRC settings to consider every supplier’s unique manufacturing limitation in hope of achieving DFM is a distinct challenge. It seems global suppliers are unwilling to share their limitations unless you send business to them. So, what are the options?

Top DFM ‘Speeding Tickets’ Issued by Suppliers

- Failure to provide design geometry to meet IPC-6012 manufacturing process and class specification
- Failure to provide tangible dimensions and tolerances defining form, fit acceptance criteria
- Failure to provide IPC-D-356 netlist (ODB++ is not utilized sufficiently offshore)
- Failure to declare copper thickness specification as “base” or “finished”
- Failure to locate an intelligent design origin relevant to the PCB such as a mounting hole
- Failure to allow for generic laminate material substitution

Where can an inexperienced designer learn more? IPC holds PCB design classes, such as

IPC[®] SYLLABUS Introduction to PCB Design I

IPC STANDARDS COVERED (PROVIDED WITH COURSE)

- IPC-2152 Standard for Determining Current Carrying Capacity in Printed Board Design
- IPC-2221 GENERIC STANDARD ON PRINTED BOARD DESIGN
- IPC-2222 SECTIONAL DESIGN STANDARD FOR RIGID ORGANIC PRINTED BOARDS
- IPC-2611 GENERIC REQUIREMENTS FOR ELECTRONIC PRODUCT DOCUMENTATION
- IPC-2612 SECTIONAL REQUIREMENTS FOR ELECTRONIC DIAGRAMMING DOCUMENTATION (SCHEMATIC AND LOGIC DESCRIPTIONS)
- IPC-2612-1 SECTIONAL REQUIREMENTS FOR ELECTRONIC DIAGRAMMING SYMBOL GENERATION METHODOLOGY
- IPC-2614 SECTIONAL REQUIREMENTS FOR BOARD FABRICATION DOCUMENTATION
- IPC-2615 PRINTED BOARD DIMENSIONS AND TOLERANCES
- IPC-4101 SPECIFICATION FOR BASE MATERIALS FOR RIGID AND MULTILAYER PRINTED

Figure 6: IPC's "drivers ed" class for designers.

those taught by Kris Moyer, as well as the CID and CID+ certification classes and exams. A variety of design classes are available at IPC APEX EXPO, DesignCon, and the PCB East and West shows. Altium's John Watson also teaches basic and advanced PCB design at Palomar College near San Diego. There are great design classes out there, and some that are not so great, so investigate the instructor's bona fides before forking over your benjamins.

IPC specifications and training courses have already laid the foundation—the prima facie—for collaborative PCB design and manufacturing specifications. They serve the global industry as a type of owner's manual for our industry systems. They are produced and represented by diverse groups of industry professionals who are subject matter experts in the PCB industry. Manufacturers aim toward these specifications to define the target conditions of our PCBs. PCB designers need

to become familiar, specify, and form their design strategies around the limits published in these documents in order to fit and function with fellow supply chain stakeholders. Designers must realize that when they create a layout without consideration for global prima facie production capabilities, they are not creating a design. They are creating an accident waiting to happen.

Now y'all have a good day and just don't drive so fast, ya hear? **DESIGN007**



Kelly Dack, CIT, CID+, provides DfX centered PCB design and manufacturing liaison expertise for a dynamic EMS provider in the Pacific Northwest while also serving as an IPC design certification instructor (CID) for

EPTAC. To read past columns, [click here](#).

Top Issues in PCB Design

CLARITY PRECEDES SUCCESS

Feature Article by Mark Thompson
OUT OF THE BOX MANUFACTURING

What are the top problems I see with PCB design? From where I sit now on the assembly side, one of my biggest concerns related to PCB design is the lack of uniform part markings on the Gerber or ODB++ data, specifically the way customers reference diodes. We would prefer either an “A” depicting the anode side or a “C” or “K” for the cathode side. Many customers simply use either a line or a dot, which requires us to contact them to clarify which side is the cathode and which side is the anode.

If a line is used to denote the cathode side, many times the silkscreen clip using the mask clearance by the fabricator wipes out most of the line, making it difficult or impossible to determine the location of the cathode side. Using a dot doesn’t really help; does a dot depict an anode or cathode? Besides, dots are typically used to denote Pin 1 designators. Please use an “A” for the anode side and a “C” or “K” for the cathode side.

Controlling Controlled Impedances

Another area that concerns me is controlled impedances. Don’t make assumptions about controlled impedances. Your goal as a PCB designer is to simulate impedance to within 10% of your goal. The fabricator should be able

to take it the rest of the way since the fabricator knows its press parameters, press values, and effective Dk. Trust your chosen fabricator and use the numbers they provide you.

If you simply go online and check material PDFs for the purpose of establishing impedances yourself be aware that many of the generic spec sheets are for very thick dielectrics (.014" core and sometimes even .028" core) the Dk associated with the thicker dielectrics are higher which, if used for trace widths .005" and below will create a mismatch and the fabricator will come back with a line size that your space may not support.

Also, consider the speed. If the literature is showing 4.5 Dk at 1 Mhz, and you know this product will be running at higher speeds, such as 5,10 or even 20 Ghz, understand the Dk will be driven way down. You may be looking at something closer to 3.8 Dk at 5 Ghz and the mismatch will affect the impedance. **DESIGN007**



Mark Thompson is an engineering manager with Out of the Box Manufacturing and a longtime CAM expert.

The 7 Core Principles of Customer Service



Source: MBA Knowledge Base (www.mbaknol.com)



MilAero007 Highlights



Nathan Edwards to Lead USPAE as New Executive Director ▶

Effective May 1, 2023, Nathan Edwards will transition into the role of executive director of the U.S. Partnership for Assured Electronics (USPAE). Currently serving as director of government development, Edwards will replace Chris Peters who will continue with the organization as a senior advisor, providing continuity and focus on special projects. As executive director of USPAE, Edwards will be responsible for establishing and growing the organization to help ensure the U.S. government has access to trusted, secure, and resilient electronics supply chains.

North American PCB Industry Sales Up 11.6% in March ▶

IPC announced the March 2023 findings from its North American Printed Circuit Board (PCB) Statistical Program. The book-to-bill ratio stands at 0.91.

Legislation Introduced to Restore America's Printed Circuit Board Industry after Two Decades of Decline ▶

The bipartisan Protecting Circuit Boards and Substrates Act of 2023 introduced by Reps. Blake Moore (R-UT-1) and Anna Eshoo (D-CA-16) finishes the job the CHIPS Act began by incentivizing investment in the domestic printed circuit board (PCB) industry.

Gardien Group Joins USPAE ▶

Gardien Group is pleased to announce its membership acceptance to the U.S Partnership for Assured Electronics.

Trackwise Awarded Prestigious King's Award for Enterprise for Innovation ▶

Trackwise Designs plc, the innovative manufacturer of specialist products using printed circuit technology, is delighted to be recognised with a prestigious King's Award for Enterprise.

Amphenol Reports First Quarter 2023 Results ▶

Sales of \$2.974 billion, up 1% in U.S. dollars and organically compared to the first quarter of 2022; GAAP Diluted EPS of \$0.71, up 4% compared to prior year; adjusted Diluted EPS of \$0.69, p 3% compared to prior year; GAAP and adjusted operating margin of 19.9% and 20.1%; operating and free cash flow of \$532 million and \$436 million.

FDH Aero Acquires BJB Electronics Group ▶

FDH Aero, a global provider of supply chain solutions for the aerospace and defense industry, has acquired BJB Electronics Group, a leading provider of interconnect and electro-mechanical products for the defense, commercial aerospace, and space end-markets.

Realizing the Promise of IPC-1791 ▶

IPC-1791, Trusted Electronic Designer, Fabricator and Assembler Requirements, is an electronics standard developed in collaboration with the (DoD) and industry to address some of today's greatest risks to a trusted supply chain. The standard provides traceability and helps protect against counterfeits. In fact, IPC-1791 was specifically cited in the U.S. Department of Commerce response to Executive Order 14017-Securing America's Supply Chains.

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Balancing Trade-offs for Optimal PCB Design

Beyond Design

Feature Column by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

The field of PCB design is evolving rapidly, which creates both opportunities and demands for new and experienced designers. PCB designers must deal with various issues in finding the right balance between the form factor, functionality, and power requirements of their boards while ensuring that the stackup, placement, and routing are completed to guarantee stringent signal and power quality. Advanced tools and skills are needed to create compact, flexible, high-performance, and low-power PCBs with faster turnaround times. There is also a trend to collaborate with other designers and manufacturers in a team environment through cloud-based platforms to ensure that the designs are reliable and manufacturable.

As multilayer PCBs become more complex, PCB designers face the challenge of cramming more components and connections onto a limited board area without compromising performance or quality. Increasing the number of signal layers can help to accommodate more signal routing and reduce crosstalk, but there are inevitable bottlenecks in the breakout of high pin-count devices. The use of high-density interconnects, blind and buried vias, and via-in-pad techniques also help to alleviate these issues.

Ball grid array (BGA) packages come in a variety of pitches and sizes. As device complexity increases and OEMs continue their drive toward smaller components, ball pitches

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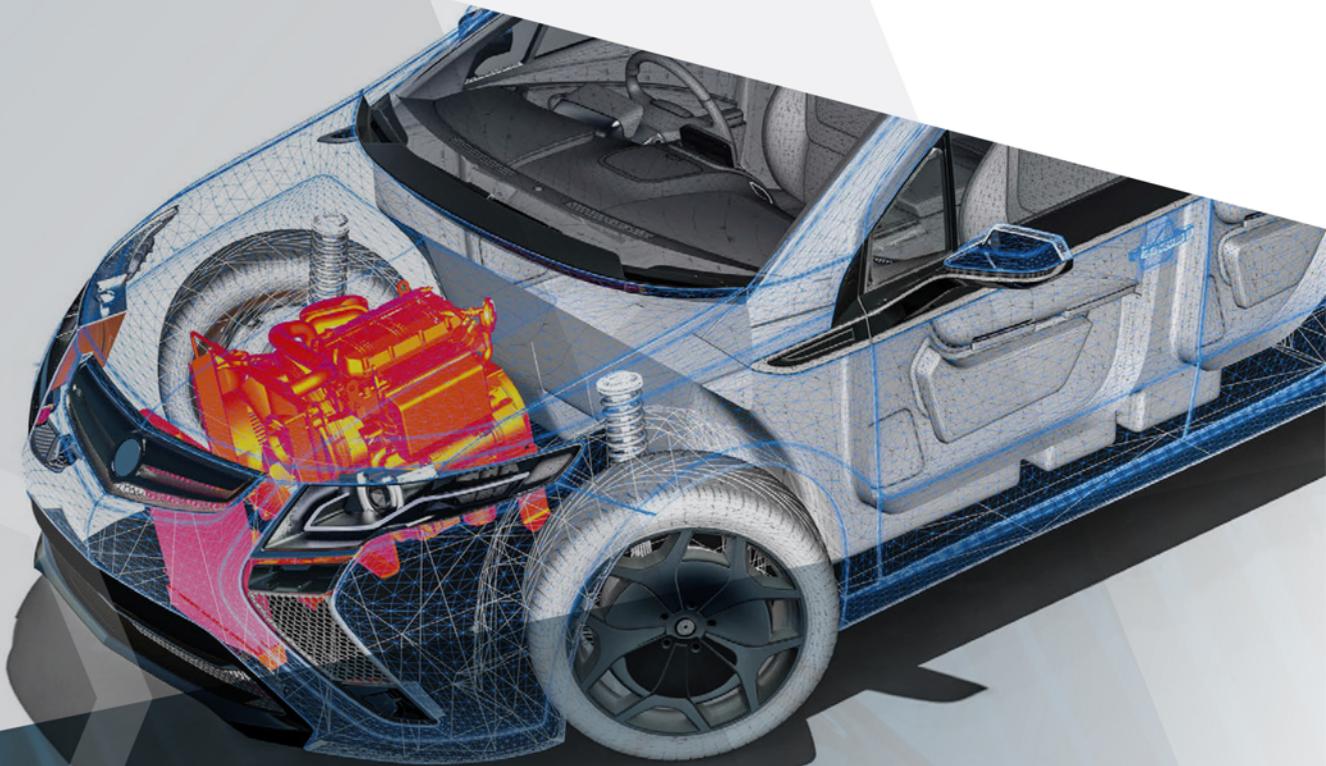
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Table 1: Typical feature sizes for BGAs. (Source: PCBLibraries)

BGA Pin Pitch	BGA Ball Dia	BGA Land Size	Land Hole Size	Plane Clearance	Trace Width	Trace/Trace Space	Trace/Via Space	Trace/Land Space	Route Grid	Part Place Grid
0.4	0.25	0.25	0.125	0.35	0.05	0.05	0.05	0.05	0.05	0.5
0.5	0.3	0.275	0.15	0.425	0.075	0.075	0.075	0.075	0.05	0.5
0.65	0.4	0.4	0.15	0.5	0.1	0.1	0.1	0.075	0.05	1
0.65	0.4	0.425	0.2	0.575	0.075	0.075	0.075	0.075	0.05	1

of 0.5 mm and lower are becoming more popular. Today, there are 0.4-mm pitch BGAs in virtually every smartphone, and 0.3-mm ultra-fine pitch BGAs are the next generation. The next step is to increase functionality within the same package. Early adopters are venturing into the 0.3-mm pitch devices. However, there are currently no formal IPC design guidelines or layout rules specifically tailored to supporting 0.3-mm pitch devices. As a result, many PCB designers largely rely on traditional 0.5-mm pitch design guidelines and layout rules to develop new 0.3-mm pitch device-based designs. For instance, the current design guidelines allow the use of a solder-ball-joint pad with a diameter of 20% less than the diameter of a BGA/CSP solder ball.

Table 1 gives an example of the required feature sizes for BGAs. This enables us to determine the signal layer count required to breakout from fine-pitch BGAs. The minimum number of signal routing layers required to route a particular design can be estimated once the location of the signals on the BGA is known.

- The first two rows/columns will route on one signal layer
- The second two rows/columns will route on a second signal layer

Plus, an additional signal layer is generally required for every row of signal balls past four rows.

This assumes that all balls are routed because their signals are needed for connectivity. But if some balls are no-connects, then those corresponding ball escape lanes are free for other

signals. In this regard, fewer layers may suffice if the required signals have enough viable routing lanes. Blind microvias and vias-in-pad are normally required for the breakout of 0.5-mm pitch or less.

Accommodating the high number of individual power supplies to the BGA is also an issue. One can generally place three to four power pours on each power layer depending on the BGA pinout. So, four power layers typically are required for 10 supplies plus ground. This could be reduced if some of the power pours are combined with signals on a mixed layer.

As the data rate increases, the bandwidth required for data transmission also increases, which poses challenges for PCB design such as signal integrity, crosstalk, impedance matching, and electromagnetic interference. The PCB designer must also balance the layer count vs. manufacturing complexity. Signal integrity requirements may also impact this decision if, for instance, parallel trace segments are over 12 mm in length with a 200 ps rise time.

PCB design is a complex and challenging task that requires designers to consider various aspects that influence the performance and quality of the PCB. Among these aspects, signal integrity, power integrity, thermal management, and electromagnetic compatibility are crucial for ensuring the functionality and reliability of the PCB. PCB designers need to acquire more knowledge and skills to analyze and optimize these aspects of PCB design using appropriate principles, methods and tools.

The increased data rates also require more complex modulation schemes for data encoding, such as non-return-to-zero (NRZ) to pulse amplitude modulation 4-level (PAM4) encoding. These schemes use multiple levels or phases of signals to encode more bits per symbol, which increases the spectral efficiency and data rate of the channel. However, these schemes also increase the complexity and sensitivity of the signal processing and recovery circuits, which require careful PCB design to ensure proper signal quality and synchronization. NRZ is a modulation technique that has two voltage levels to represent logic 0 and logic 1. While PAM4 uses four voltage levels to represent four combinations of 2-bit logic: 11, 10, 01, and 00 (Figure 1).

Impedance is the key factor that controls the stability of a design. It is the core issue of the signal integrity methodology. The impedance should be simulated by a field solver to obtain accurate values of impedance for each signal layer of the substrate. The impedance of the trace is extremely important, as any mismatch along the transmission path will result in a reduction in the quality of the signal and possible radiation of noise. For perfect transfer of energy, the impedance at the source must equal the impedance at the load.

However, this is not naturally the case and terminations are generally required at fast edge rates to limit ringing. If this noise is not constrained at the source, then it will be coupled into nearby victim traces (crosstalk) and

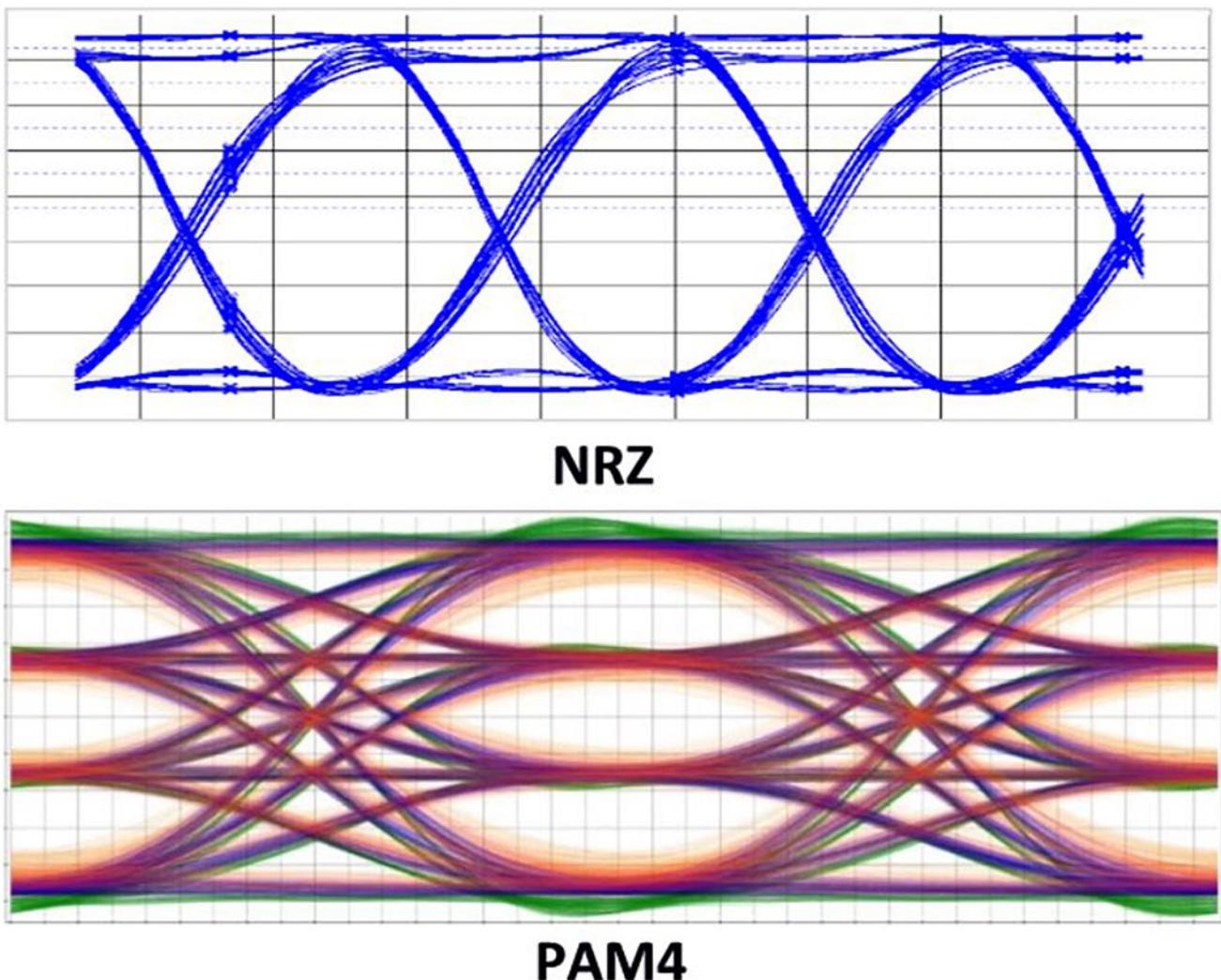


Figure 1: NRZ eye vs. PAM4 eye. (Source: Xilinx)

radiate to create more EMI. Apart from the issues of EMI, signal integrity, and crosstalk, this noise can cause intermittent operation of the product due to timing glitches and interference, dramatically reducing the reliability of the product. Excessive ringing can also lead to power integrity issues.

Flight time delay and skew are the key pillars in high-speed PCB design signal integrity. One of the driving factors for flight time and skew performance is the placement of components. In the classic high-speed design flow, timing specifications simulation results are compared to determine placement and routing constraints. Given a length constraint, a designer can control signal integrity by controlling the PCB trace topology of the various parts of an interface. Included in this topology are any terminations. Figure 2 shows an eye diagram of a signal with jitter and ringing due to poor termination.

The integrity of the PCB stackup and the PDN are the basis for a stable product. Multi-

layer PCB design is becoming more complex and less forgiving—it's not just about signal integrity, crosstalk, and EMI. The substrate and the power delivery system are extremely critical and if they should fail then the whole system can go down or, in the worst case, may just work intermittently.

Today's high-performance processors employ low DC voltages with high transient currents and high clock frequencies to minimize power consumption and hence the amount of heat dissipated. A typical high-speed design contains 10 or more individual power supplies. And unfortunately, the lower core voltages, higher currents, and faster edge rates all impact the power distribution network (PDN) design, as well as signal integrity.

Ideally, the effective impedance of the PDN should be kept below the target impedance up to the maximum required bandwidth. However, if the impedance is too far below the target, then this implies that the PDN has been overdesigned which unnecessarily increases

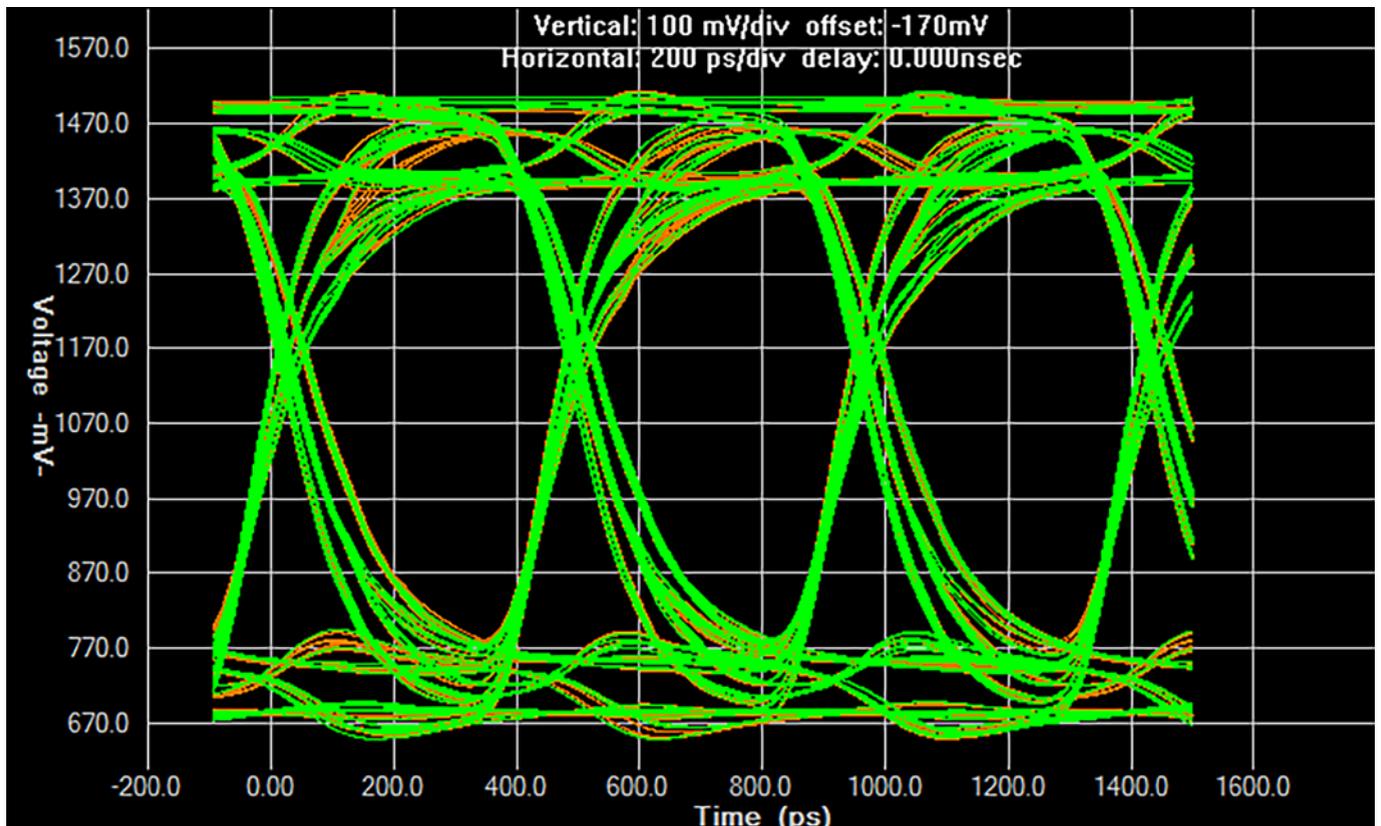


Figure 2: Eye diagram of a signal with poor termination.



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costs with little added benefit. If your company intends to build hundreds of thousands of assemblies, then the potential cost saving can be quite significant. Analyzing the PDN ensures the best performance at the most cost-effective price.

Many competent PCB designers will retire within the next few years leaving a void in the knowledge base. This creates a shortage of skilled and experienced PCB designers, increases the demand for new and young PCB designers, and allows for more opportunities for collaboration and innovation among PCB designers. However, the lack of manufacturing knowledge of the upcoming designers can cause design errors and failures, increase the design time and cost, and reduce the manufacturability and yield of the product.

Experience is the best teacher of all. PCB designers need to have more knowledge and skills to design PCBs that have high signal integrity, power integrity, thermal performance, and electromagnetic compatibility. PCB designers must understand the principles, methods, and tools for analyzing and optimizing all aspects of PCB design.

Key Points

- PCB designers must deal with various issues in finding the right balance between the form factor, functionality, and power requirements of their boards.
- BGA pitches of 0.5 mm and lower are becoming more popular.
- 0.3-mm ultra-fine pitch BGAs and increased functionality within the same package are the next generation.
- Currently there are no formal IPC design guidelines or layout rules specifically tailored to supporting 0.3-mm pitch devices.
- Blind microvias and vias-in-pad are normally required for the breakout of 0.5 mm pitch or less.
- Accommodating the high number of individual power supplies to the BGA is also an issue.

- The increased data rates also require more complex modulation schemes for data encoding, such as non-return-to-zero (NRZ) to pulse amplitude modulation 4-level (PAM4) encoding.
- The impedance should be simulated by a field solver to obtain accurate values of impedance for each signal layer of the substrate.
- Flight time delay and skew are the key pillars in high-speed PCB design signal integrity.
- The integrity of the PCB stackup and the PDN are the basis for a stable product.
- The lower core voltages of today's processors require higher currents and faster edge rates.
- The effective impedance of the PDN should be kept below the target impedance up to the maximum required bandwidth.
- If the impedance is too far below the target, then this implies that the PDN has been overdesigned which unnecessarily increases costs with little added benefit.

DESIGN007

Resources

- Beyond Design by Barry Olney: "Fly-over Technology: When It All Gets Too Fast," "Signal Integrity (Parts 1 & 3)," "The Target Impedance Approach to PDN Design."
- AM57xx BGA PCB Design, Texas Instruments.
- "Metric Pitch BGA and Micro BGA Routing Solutions" by Tom Hausherr.



Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD

Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded at www.icd.com.au. To read past columns, [click here](#).



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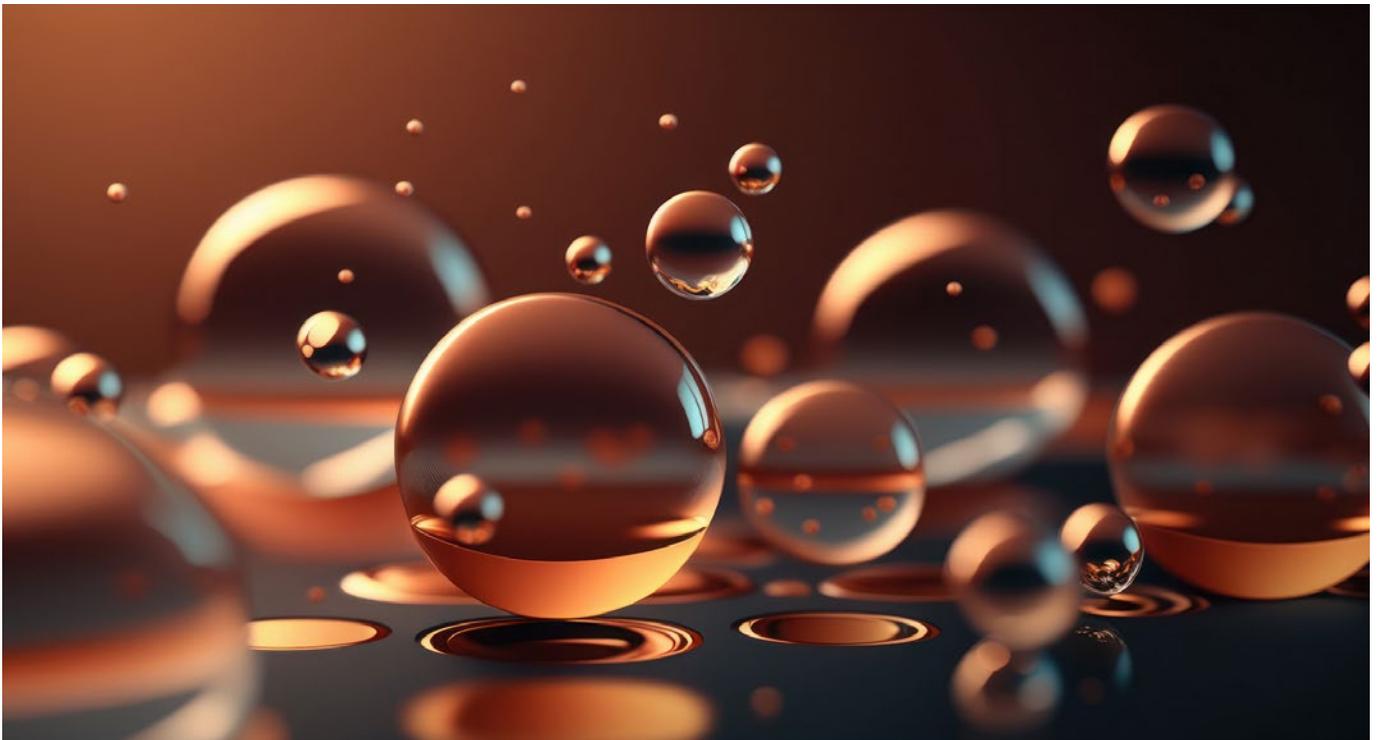
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Reassessing **Surface Finish Performance** for Next-generation Technology, Part 1

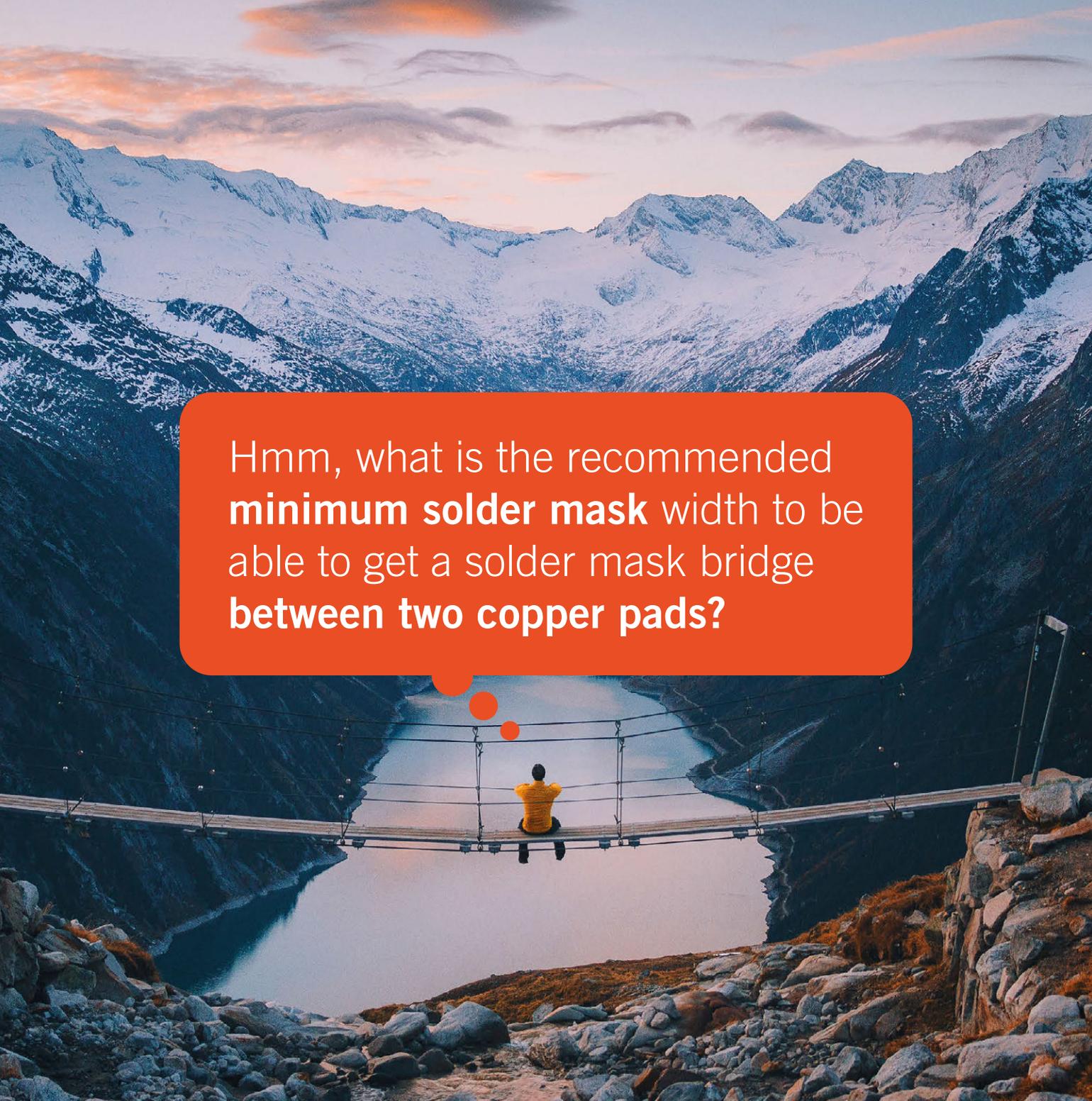
Article by Frank Xu, PhD
and Martin Bunce, MACDERMID ALPHA,
and John Coonrod, ROGERS CORPORATION

Introduction

Over the years, various surface finishes have been successfully utilized, namely organic solderability preservative (OSP), immersion silver (ImAg), immersion tin (ImSn), electroless nickel immersion gold (ENIG), and electroless nickel electroless palladium immersion gold (ENEPIG), as solderable finishes for PCB and package substrates. All these surface finishes have their pros and cons, with no single finish being suited to all applications.

As system designers continue to respond to new performance demands, it can be noted that ENIG/ENEPIG finishes have endured as a leading choice in many advanced applications where reliability is prioritized over cost.

Electroless nickel (EN) deposits have served well as a barrier layer, preventing copper migration to the outer gold or palladium-gold surfaces, and enabling the robust solderability performance of ENIG and ENEPIG finishes. However, the introduction of the 5G mobile network creates a growing demand for smartphones, networking, and wireless connections, all requiring increased “data flow.” The need to reduce the signal loss at higher frequency bandwidth is becoming vitally important. The low conductivity and magnetic properties of EN affect electrical signals as they travel along a conductor’s outer surfaces leading to insertion losses at higher frequencies.

A person in a yellow shirt is sitting on a suspension bridge that spans across a deep valley. The bridge is made of wooden planks and is supported by cables. Below the bridge is a calm lake that reflects the surrounding mountains. The mountains are covered in snow and are very high. The sky is a mix of blue and orange, suggesting a sunset or sunrise. The overall scene is peaceful and scenic.

Hmm, what is the recommended **minimum solder mask** width to be able to get a solder mask bridge **between two copper pads**?

PCBs are complex products which demand a significant amount of time, knowledge and effort to become reliable. As it should be, because they are used in products that we all rely on in our daily life. And we expect them to work. But how do they become reliable? And what determines reliability? Is it the copper thickness, or the IPC Class that decides?

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As a result, designers and fabricators are looking for newer-generation surface finishes to meet their performance criteria. EPIG (electroless palladium immersion gold with no EN), silver-gold (Ag-Au), and reducing the EN thickness from traditional ENEPIG, have all gained attention. What follows is a review that compares the performance attributes of the leading candidates for a high-frequency alternative surface finish.

MacDermid Alpha Electronic Solutions has worked in partnership with Rogers Corporation to evaluate the effect of various surface finishes on signal loss with increasing frequency. Together, we subsequently worked to understand and compare other critical-to-quality performance metrics that will guide application-based surface finish selection.

Work Program

We first set out to evaluate the effect of surface finish on signal losses up to 110 GHz using the microstrip test method and a vector network analyzer, with the support of Rogers.

The test candidate surface finishes selected are:

- Standard ENEPIG (4 μm electroless nickel/0.1 μm palladium/0.05 μm gold)
- Standard ENIG (4 μm electroless nickel/0.05 μm gold)-
- Thin EN ENEPIG (0.2 μm electroless nickel/0.1 μm palladium/0.05 μm gold)
- Ultra-Thin EN ENEPIG (0.1 μm electroless nickel/0.1 μm palladium/0.05 μm gold)-
- EPIG (0.1 μm palladium/0.05 μm gold)-
- Ag-Au (0.15 μm silver/0.05 μm gold)
- Immersion Silver (0.3 μm)
- OSP (0.4 μm)

Following the evaluation of insertion losses, each surface finish was assessed based on other performance criteria:

- High-speed ball shear
- Solder spread testing
- Drop shock evaluation

- Gold and aluminum wire bonding
- Solder joint electromigration

After data collection, it was summarized, and a decision matrix was constructed to allow designers to compare performance requirements against each surface finish's capabilities.

Insertion Loss Testing

The total insertion loss through a microstrip circuitry, α_T , comprises four different loss components as shown in Equation 1:

$$\alpha_T = \alpha_D + \alpha_C + \alpha_R + \alpha_L$$

where α_D , α_C , α_R , and α_L represent the dielectric loss, the conductor loss, the radiation loss, and the leakage loss, respectively. If the transmission line is an ideal impedance-matching circuit, the total transmission loss can be expressed using only two dominant factors, i.e., the conductor and dielectric losses, as shown in Equation 2¹.

$$\alpha_T = \alpha_D + \alpha_C$$

Multiple factors affect the conductor loss of the transmission line, including surface roughness of the copper foil, skin effect, and magnetic permeability of the conductor. The skin effect is closely related to the surface finishes. When the frequency of the signal increases, the current flowing in the transmission line focuses on the surface of the copper foil, instead of the center of the foil. This is known as the skin effect. The skin depth δ amplitude of the current flowing on the surface of the transmission line can be derived using Equation 3 below^{2,3}.

$\delta = \sqrt{\frac{1}{\pi f \mu \sigma}}$ <p>f = frequency μ = permeability σ = conductivity</p>	<p>Approximate conductivities (σ) of metals</p> <table border="0"> <tr><td>Silver</td><td>6.301 x 10⁷ S/m</td></tr> <tr><td>Copper</td><td>5.817 x 10⁷ S/m</td></tr> <tr><td>Gold</td><td>4.520 x 10⁷ S/m</td></tr> <tr><td>Nickel</td><td>1.500 x 10⁷ S/m</td></tr> <tr><td>Tin</td><td>0.870 x 10⁷ S/m</td></tr> <tr><td>Solder</td><td>0.700 x 10⁷ S/m</td></tr> </table>	Silver	6.301 x 10 ⁷ S/m	Copper	5.817 x 10 ⁷ S/m	Gold	4.520 x 10 ⁷ S/m	Nickel	1.500 x 10 ⁷ S/m	Tin	0.870 x 10 ⁷ S/m	Solder	0.700 x 10 ⁷ S/m
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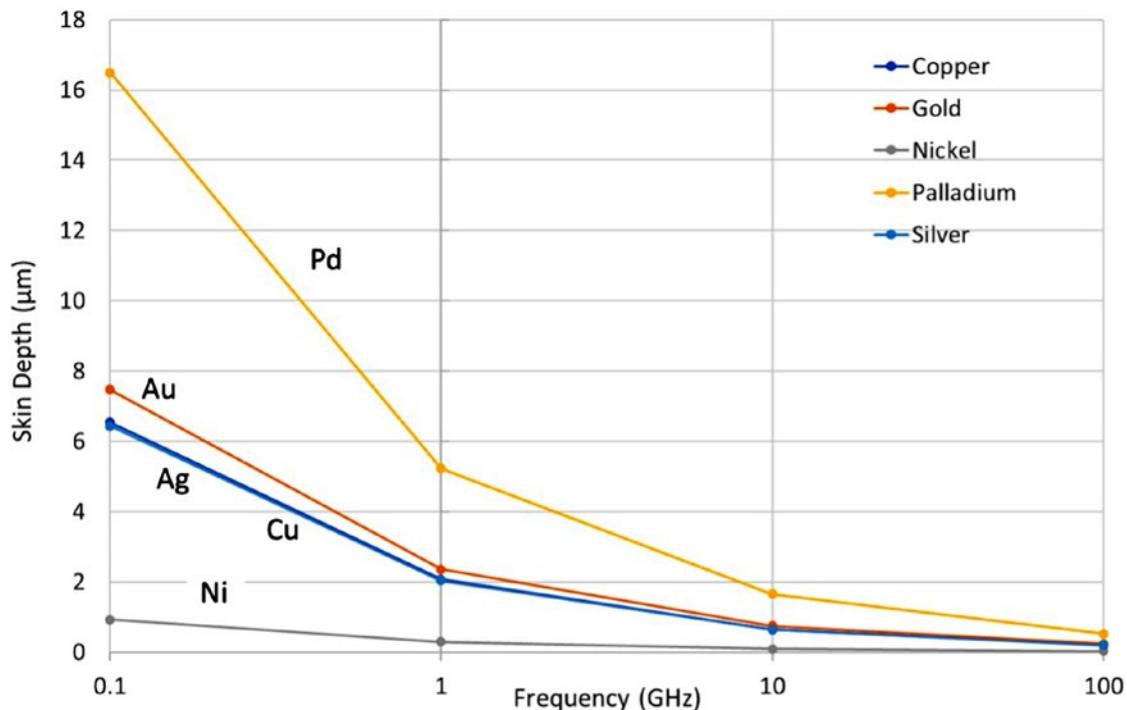


Figure 1: Skin depth in Cu and other plated finishes.

Figure 1 shows the skin depth of copper (Cu) and the plating material of fabricated transmission lines⁴. The results demonstrate that Pd had the deepest skin depth, followed by gold (Au), silver (Ag), copper (Cu), and nickel (Ni). Ni, which is ferromagnetic, with the highest magnetic permeability, has a shallow skin depth, whereas a low electrical conductivity, Pd, has improved skin depth. At 1 GHz, the skin depth of Ni is less than 0.5 µm.

MacDermind Alpha worked in collaboration with Rogers on the signal loss testing. Figure 2 is a Rogers signal loss test vehicle drawing. It contains identical top and bottom halves. To test the surface finish contribution in signal loss testing, the test vehicle is cut in half. One half is coated with the

finish of interest while the other half remains uncoated. Both halves are subject to signal loss testing. The difference between the two signal loss results equals the loss from the surface finish. The data on the uncoated board is called

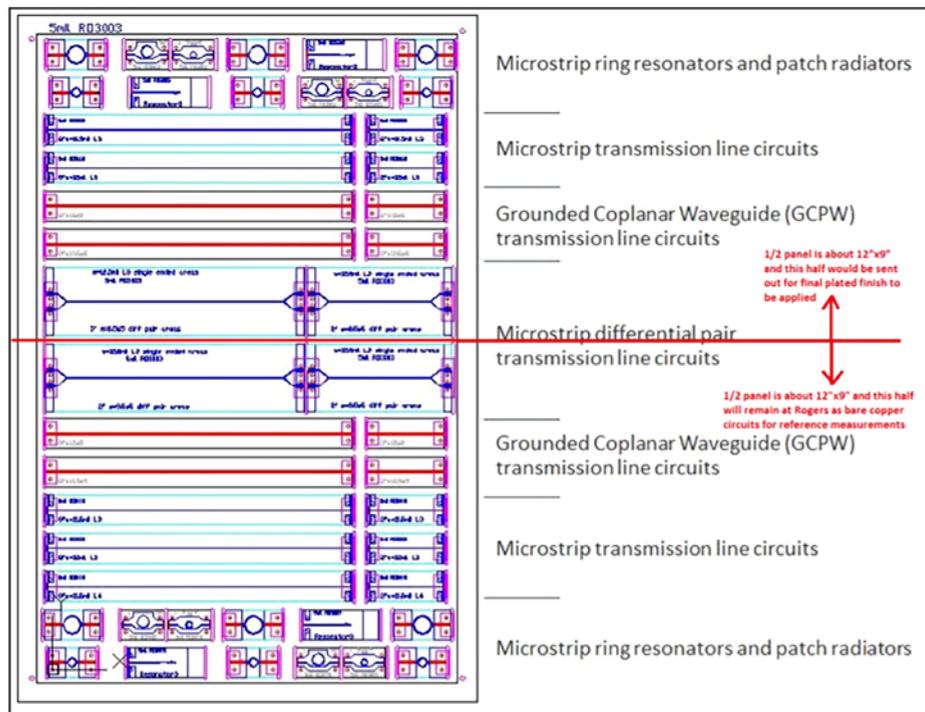


Figure 2: Rogers signal loss test of a vehicle consisting of identical top and bottom halves.

the construction loss. By conducting this test, the panel-to-panel variation is mitigated.

Insertion Loss Data

To simplify data analysis, a stacked bar chart was constructed (Figure 3), focusing on three frequencies commonly used in real-world applications.

- 6 GHz: Standard operation
- 40 GHz: 5G
- 77 GHz: ADAS

The stacked bar includes two components. First, the blue bar represents loss due to the construction of the test vehicle (the data obtained using the copper-only half of the test vehicle). Second, the red bar shows the additional loss due to surface finish application to the second half of the same test vehicle. Thus, the total height of the bar represents the total loss for construction and finish.

Insertion Loss Data Analysis

Minor differences in the height of the blue bars (construction loss) can be observed at each frequency in Figure 3.

In a perfect world, we would hope to observe the same signal loss from each of the copper-only test vehicles. However, experimental errors are possible, reducing repeatability between tests. The variance observed between the construction-only losses is believed to be due to either signal loss measurement error or, more likely, minor differences in the construction (etched definition, trace uniformity, surface roughness, etc.) between the individual test vehicles. These differences are small enough to allow effective judgment and comparison of signal losses for each surface finish.

Once taking into consideration the minor experimental variance, it is possible to categorize the surface finish test candidates into three categories:

Category 1

OSP and immersion silver are shown to add no additional signal loss over the construction sample. Silver is a better conductor than copper while OSP is an ultra-thin organic coating; both finishes have no detrimental effect on the signal loss.

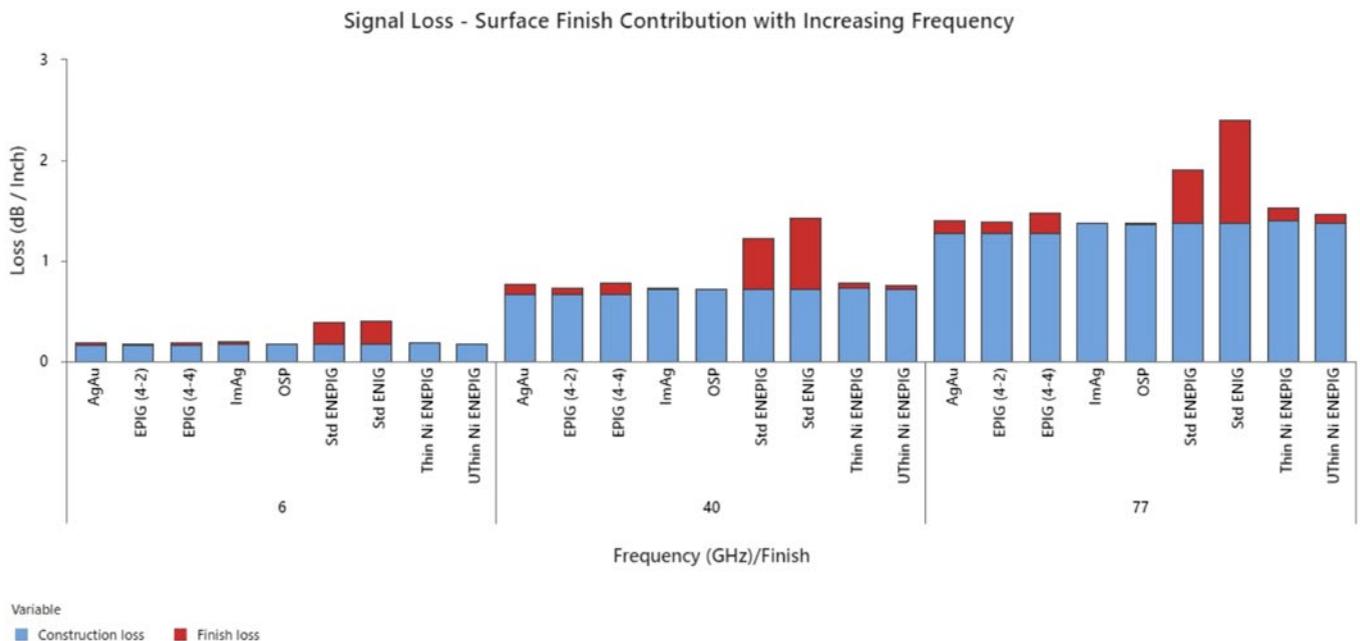
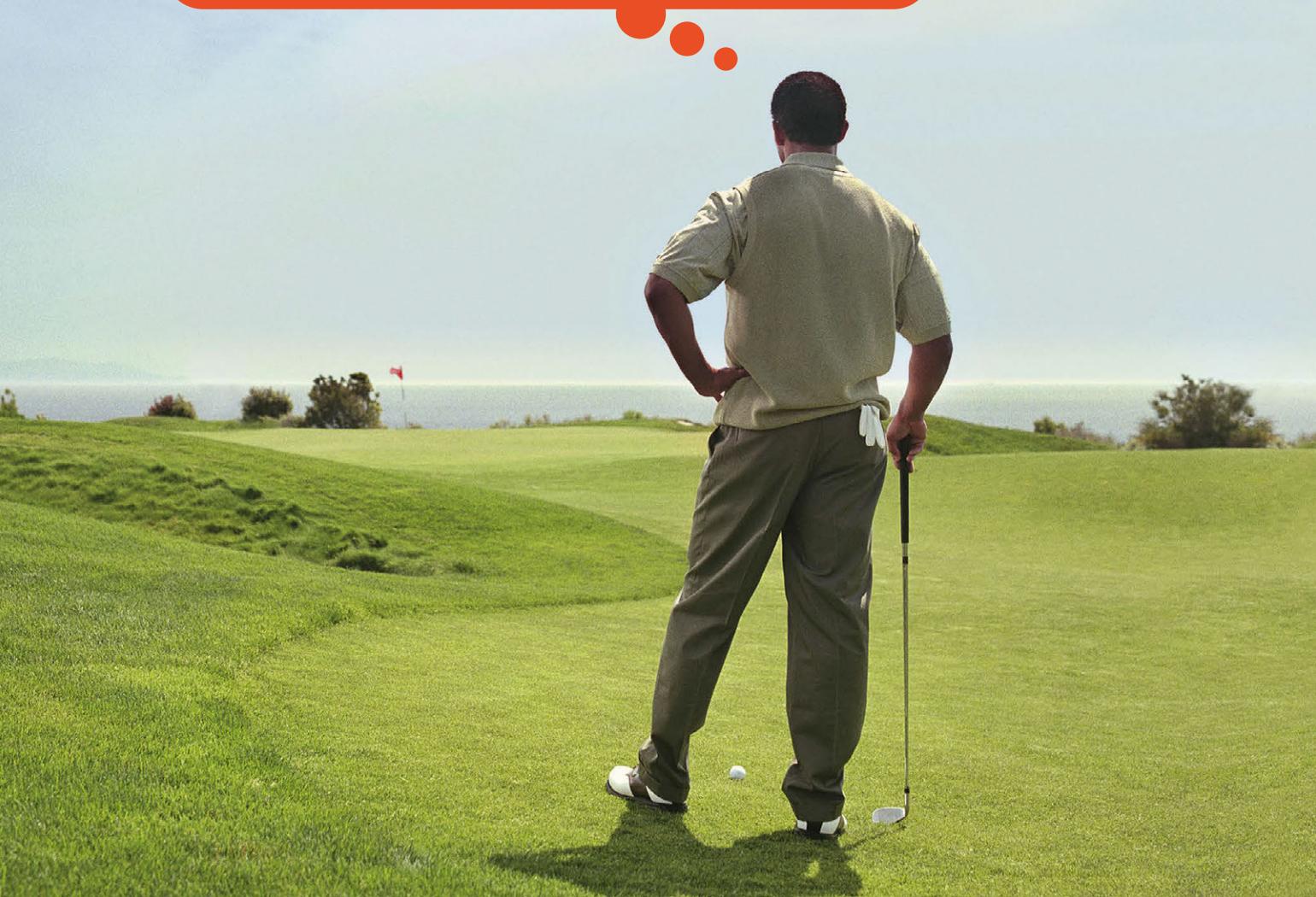


Figure 3: Signal loss due to construction (blue) and surface finishes (red) at representative frequencies.

Hmm, what is recommended
**minimum distance for
copper to board edge?**



PCBs are complex products which demand a significant amount of time, knowledge and effort to become reliable. As it should be, because they are used in products that we all rely on in our daily life. And we expect them to work. But how do they become reliable? And what determines reliability? Is it the copper thickness, or the IPC Class that decides?

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OSP and immersion silver are proven to be the best surface finish options for optimal performance with high-frequency operation.

Category 2

ENIG and ENEPIG with typical (4 μm EN) thickness show significant signal losses over the construction compared to all other test candidate finishes. As previously stated, the magnetic and low conductivity of the thick EN deposit place limits on suitability for high-frequency operation.

Category 3

Silver-gold, EPIG, and reduced nickel thickness ENEPIG options all showed a similar insertion loss response with increasing frequency. It is therefore difficult to say if any of these three finishes are significantly different in performance.

It was surprising to find that the total elimination of the EN layer with the EPIG and silver-gold options did not outperform finishes with a very thin EN layer.

Despite not showing the perfect high-frequency performance of OSP and immersion silver, the Category 3 finishes were able to demonstrate significant improvements in insertion loss over ENEPIG and ENIG and may well bring other performance advantages not realized with OSP and immersion silver.

Conclusion

ENIG and ENEPIG are challenged by signal losses at higher frequency, with OSP and immersion silver demonstrating no losses over the construction.

The new generation surface finishes (Ag-Au, thin EN-ENEPIG, and EPIG) continue to outperform traditional ENIG and ENEPIG. Other selection criteria, such as environmental resistance, soldering performance, solder joint reliability, and wire bonding, make these newer finishes attractive for certain applica-

tions where OSP and silver cannot meet performance needs.

Our next article will be a data-driven review, examination, and comparison on high-speed ball shear, drop shock, wirebonding, and solder joint reliability performance of the newer generation and traditional surface finishes. A decision matrix will be included to assist designers in aligning performance needs with surface finishes capabilities. **DESIGN007**

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Martin Bunce is product director for MacDermid Alpha Electronics Solutions.



John Coonrod is technical marketing manager for Rogers Corporation.

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Avoiding Five Common Pitfalls of Parts

Connect the Dots

Feature Column by Matt Stevenson, SUNSTONE CIRCUITS

Ill-fitting parts can frequently cause delays and cost overruns, and undermine PCB performance, durability, and overall quality of the board. These poor results can be avoided. Here are five methods designers can implement to avoid common, parts-related manufacturability pitfalls.

1. Pay close attention to pinhole size

It's important to check component physical dimensions, consider dimension tolerances, and account for variation that can affect fit. Pins can be the wrong size or have the wrong spacing, and components can be much larger than their footprint or land pattern might indicate.

Alternate or replacement components can be on the wrong end of the tolerance range. It just takes a few mils before things don't fit and

assembly starts to go wrong. Finding a good alternate part can be a challenge, which is why datasheets are invaluable.

In addition to watching part sizes, pay close attention to the minimum, nominal, and maximum material conditions for the original part.

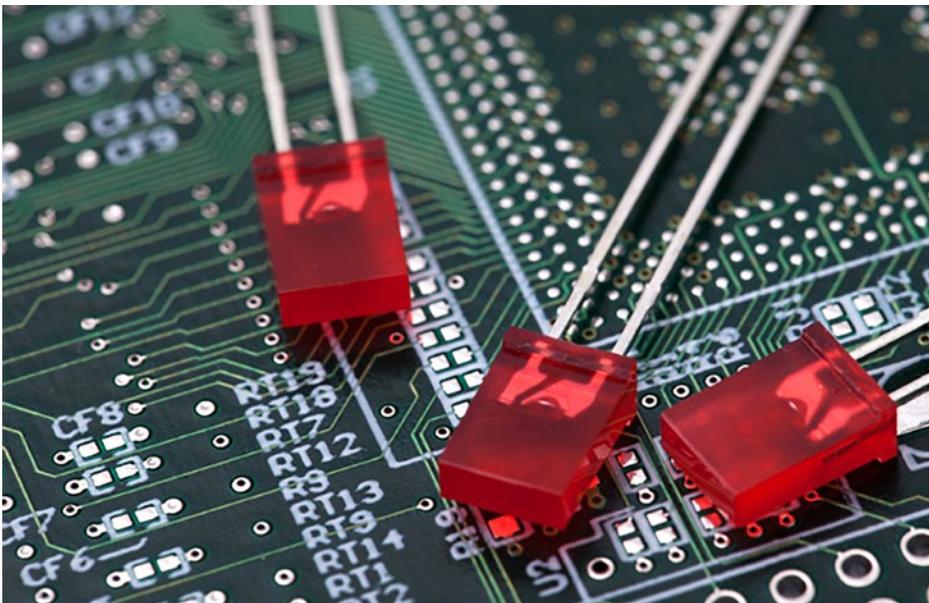
2. Use the product datasheet when designing the land pattern

One of the most frustrating mismatches with alternate through-hole parts is when the land pattern matches, but the pin size is off.

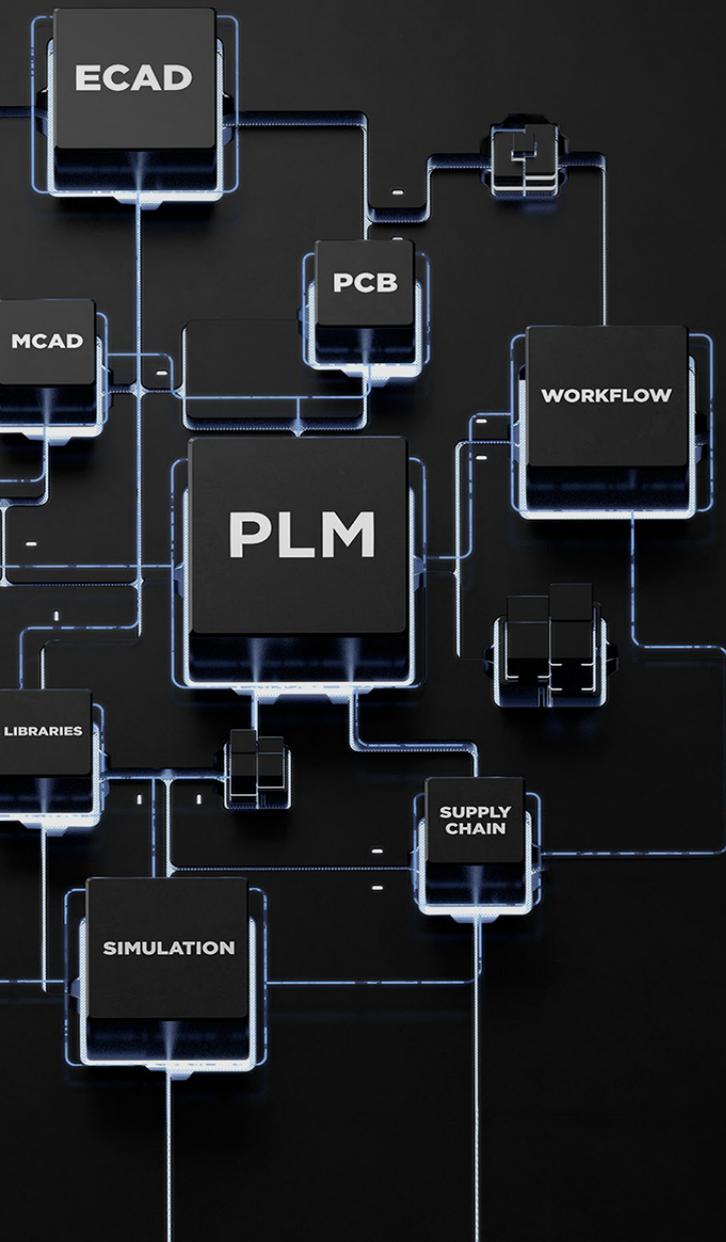
If hole sizes are too tight, pins may not fit through the holes. Or, if pins do go into the holes, they may not solder well. Solder will need to flow up through the gap between the pin and the hole barrel. If there is not enough space to allow solder mass to flow through the hole, the circuit board will absorb heat from

the molten solder and cause the solder to solidify part way up the hole. This "cold" solder joint can result in premature failure of your circuit.

When designing the land pattern, the pin size and tolerance range for components can be found in the product datasheet. Use that information to plan the proper hole size. Component holes should be sized correctly to allow



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between 12- and 16-mils diameter larger than the component pin at maximum material condition (MMC).

MMC is the condition where the hole is drilled at the low end of the tolerance range, and the pin measures at the high end of the tolerance range. Pin locations should be placed at nominal location, or the basic dimension shown on the datasheet.

3. Let the datasheet tell the real story

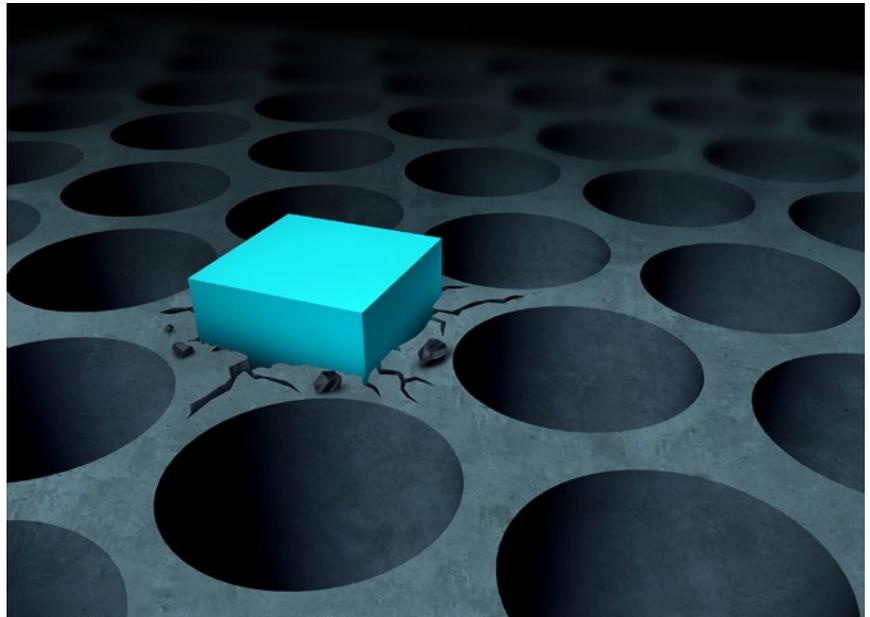
Third-party CAD libraries can contain millions of different parts, so discrepancies are inevitable. When the datasheet and the library part don't match, address the delta before submitting the design. Always check any library part for accuracy before using it the first time.

The datasheet for a part usually tells the real story—a long story, but one worth reading. Some datasheets can run up to 200 pages, but only a few lines provide the information needed to make the crucial decisions about sizing. It's important to read and comprehend the key parts of datasheets so problems in CAD don't lead to the wrong sizing and spacing on the PCB.

4. Pay attention to pinouts when using alternate vendor parts

Even if pin size and through-hole size are a confirmed match, and even if solder joints appear sound, a part can still not work as expected. Similar parts with the same footprint might look like they should act identically, but they won't always have the same pinout. Each transistor has a gate, drain, and source, but different manufacturers can vary in what goes where. For example, a Motorola part can differ from a Texas Instruments part.

When it comes to generics, there is even more potential for variance. The same basic



component will come in multiple packages. Sometimes the variations are tossed into the back of a datasheet as an afterthought, but these can be critical. Similarly named packages can even come in different widths.

5. Be aware of mechanical fit

It's not just the footprint and through-holes that are important; physical size of a component can keep parts from fitting into designated spaces. MMC body size should be the rule, so pay close attention to the tolerance range.

As parts get larger or are sourced from multiple vendors, footprint size may need to expand considerably to accommodate all of the dimension and tolerance variables. When combining multiple part body dimensions, always take the largest dimension or it may become more possible for parts to end up smashed together on the board.

Maintaining awareness of these key areas will help ensure parts-related manufacturability issues are avoided. **DESIGN007**



Matt Stevenson is vice president at Sunstone Circuits. To read past columns, [click here](#). Matt is also the author of the popular book, *The Printed Circuit Designer's Guide to... Designing for Reality*.

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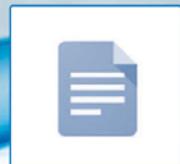
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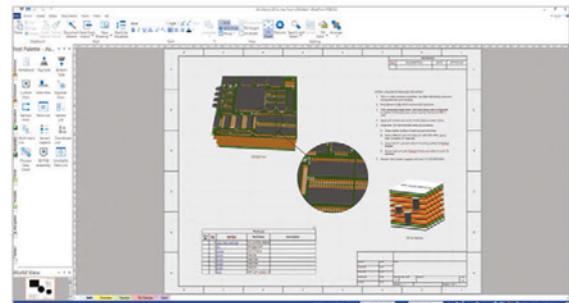
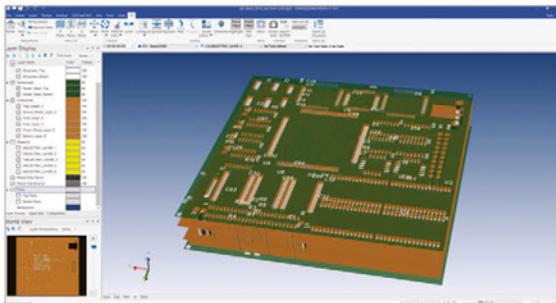
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Millimeter-wave Properties and PCB Design Challenges

Lightning Speed Laminates

by John Coonrod, ROGERS CORPORATION

Design considerations for RF PCBs can vary greatly. Many of the newer RF PCB designs are intended to accommodate millimeter-wave (mmWave) technology and as mmWave chipsets continue to diversify, there are some things that will remain the same for these applications. Understanding the basic needs of circuit design, which are good for mmWave performance when using PCB technology, can be advantageous to the circuit designer.

PCB design attributes greatly influence RF performance, particularly in relation to frequency. Low- and high-frequency applications require different PCB design disciplines. As a general statement related to this article, the comments about lower frequency are typically at 10 GHz or less. Millimeter-wave frequencies are defined to be approximately 30 GHz to 300

GHz and this article will focus more attention on mmWave applications from about 40 GHz to 90 GHz.

Considering Wavelength

Wavelength is a critical consideration for mmWave design. For those who are less familiar with RF technology, wavelength can be confusing, but there are some general definitions that can clarify the topic. It is easier to think about wavelength in physical terms, instead of the more detailed electromagnetic definitions. Wavelength is as the name implies: the physical length of a wave. To give some examples with comparisons for a PCB may be helpful.

As an example, using a simple double-sided circuit that is microstrip (signal conductor on



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top, ground plane on bottom), with a 5-mil thick dielectric material that has a Dk of 3, the length of the wave on that circuit when operating at 2 GHz is approximately 3.9 inches (99.1 mm). If the frequency doubles to 4 GHz, the length of the wave will be twice as small and would be ~ 1.95" (49.5 mm). A higher frequency will give a wave of shorter length. When considering 60 GHz for this example, the wavelength is about 0.13" (3.3 mm).

Here is another way to think about wavelength: If the circuit has a special conductor feature that is 0.26" (6.6 mm) in length, then at 60 GHz that circuit feature will have two full waves propagating on it and it can be said the circuit length is two wavelengths.

If the circuit feature is changed to be much shorter and is 0.065" (1.65 mm) in length, that conductor can be defined in terms of wavelength as a half-wavelength conductor when operating at 60 GHz.

As a quick reminder, the waves that propagate on the PCB can be thought of as sine waves; a sine wave is made up of 360 degrees. If the propagating wave on a circuit encounters an anomaly, like a circuit etching defect, some portion of the wave will be affected by that anomaly. If the anomaly is small and it only affects 10 degrees of the propagating wave, then the wave will not be distorted much, and the circuit will perform as expected. If the anomaly is much larger and can affect 90 degrees of the propagating wave, the wave will have some distortion and the circuit will probably not perform as expected.

The idea of the physical length of the conductor, as it relates to the physical length of the wave (wavelength), is critical for understanding why mmWave circuits need to be manufactured with much more precision than circuits operating at lower frequency. Again, looking

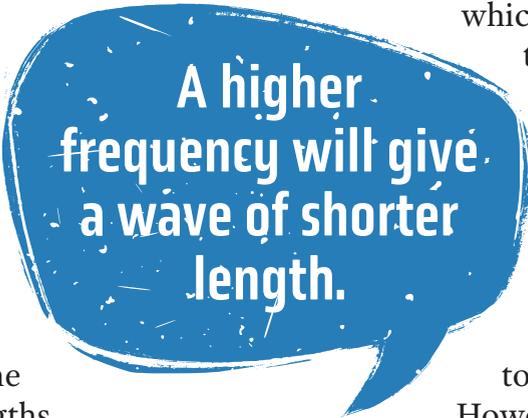
at some of the example comparisons, if a circuit is operating at 2 GHz with a wavelength of about 3.9" (99.1 mm) and the circuit has an etched anomaly about 0.033" (0.84 mm) in length, that will equate to about 3 degrees of the wave being affected and that will not cause a difference in the overall wave performance.

However, that same anomaly for a circuit operating at 60 GHz will be equivalent to about 90 degrees of the propagating wave, which is a significant portion of the wave. The wave properties will be distorted, and the circuit will not perform as expected.

The examples given here are relatively simple and meant to help the thought process.

However, there are a lot of special conductor geometries which the RF engineer will purposely design for the circuit performance they want. The propagating wave will be much more sensitive to some of these special conductor geometries and very small differences in the geometry can make big differences in circuit performance. For radar circuits operating at 77 GHz, there have been notable RF performance differences due to certain circuit geometry varying as little as just a few mils.

The PCB designer working with applications at different frequencies should be mindful of circuit feature sizes as it relates to the wave size (wavelength) and consider the possible variations of circuit geometry due to the PCB fabrication process. **DESIGN007**



A higher frequency will give a wave of shorter length.



John Coonrod is technical marketing manager at Rogers Corporation. To read past columns, [click here](#).

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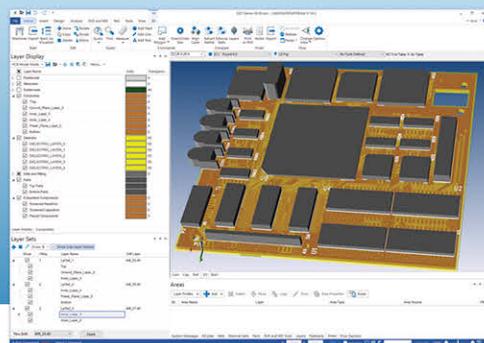
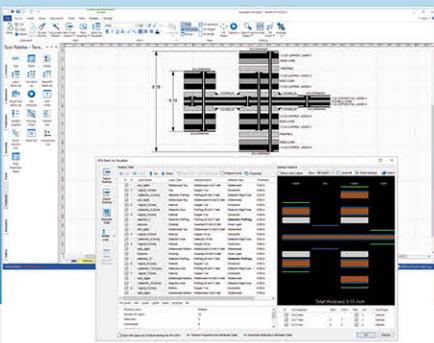
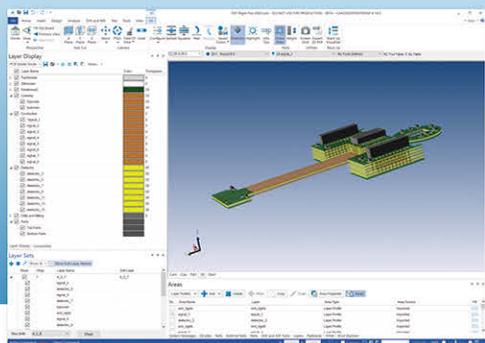


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Flex007 Highlights



New Flex Circuits Guide Now Available From American Standard Circuits ▶

I-Connect007 and American Standard Circuits are proud to announce the launch of the companion guide to the immensely popular book, *The Printed Circuit Designer's Guide to... Flex and Rigid-flex Fundamentals*. This short guide is designed to provide additional insights and best practices for those who design or manufacture flex and/or rigid-flex circuit boards. Download your free copy today at: [I-007ebooks](#).

Flexible Printed Circuit Boards Market to Reach \$20B by 2029 ▶

Maximize Market Research has published a competitive intelligence and market research report on the "Flexible Printed Circuit Boards Market." The total Flexible Printed Circuit Boards Market revenue is expected to grow at a CAGR of 10.725 percent from 2023 to 2029, reaching USD 40.81 billion during the forecast period.

Selecting Flex Materials: Do Your Homework ▶

While the layout of the circuit gives us much of the electrical characteristics of the design, your choice of materials can affect the mechanical and electrical characteristics of the circuit. Material choices affect not only the design of the circuit for its environment, but also the manufacturing and assembly processes.

Challenges of DFM Analysis for Flex and Rigid-flex Design, Part 2 ▶

While less common in rigid PCBs, flexible PCBs have many inter-layer dependencies that,

if not managed well, may lead to manufacturing issues or field failures.

NextFlex Calls for 3D Imaging Technology Proposals ▶

Nolan Johnson talks with Scott Miller about a special "Open Project" call for proposals which NextFlex currently is exploring for methods to dewarp 3D scans of physical boards to enable multi-image scans to be stitched together. There is the possibility of funding for viable proposals.



SEMI Flextech Invites Proposals for Flexible Hybrid Electronics Innovations ▶

FlexTech has issued a request for proposals (RFP) for advances in materials, FHE design tools, additive-enabled processing, hybrid electronics packaging, FHE manufacturing, AI/ML applications, soft robotics, and power solutions. Selected projects will receive cash awards ranging from \$250,000 to \$1 million. The program is funded by the Army Research Laboratory (ARL).

Take your flex game to the next level

This guide provides additional insights and best practices for those who design or utilize flex and/or rigid-flex circuit boards.



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Challenges of DFM Analysis for Flex and Rigid-Flex Design, Part 3

Article by Mark Gallant

DOWNSTREAM TECHNOLOGIES

(Editor's note: This is the final installment of a three-part series. To read Part 2, [click here](#).)

What a True Rigid-flex DFM Analysis Solution Must Include

DFM analysis tools for the last several decades have focused on a typical rigid PCB or some variant. While many standard DFM constraints are applicable, flex has many unique requirements that cannot be addressed with typical DFM analysis. Flex and rigid-flex DFM must be targeted toward the unique materials and processes used to produce flex and rigid-flex designs.

One such example is board outline vs. layer profile. Some CAD systems do not support boundaries on a per layer basis. For most rigid-flex designs, all that is provided is a cumula-

tive board outline that is the extent of all layer shapes. Without a defined boundary per layer, there may be no prevention of routing traces or placing components outside, or off of, a layer in the CAD system. The CAD DRC may also miss these items because they are within the boundary of the cumulative board outline. Having a DFM tool capable of analyzing each layer against its unique profile can detect when conductors are outside, or off of, their respective layers.

Here is a categorized list of the types of analyses and features a flex or rigid-flex DFM tool should have.

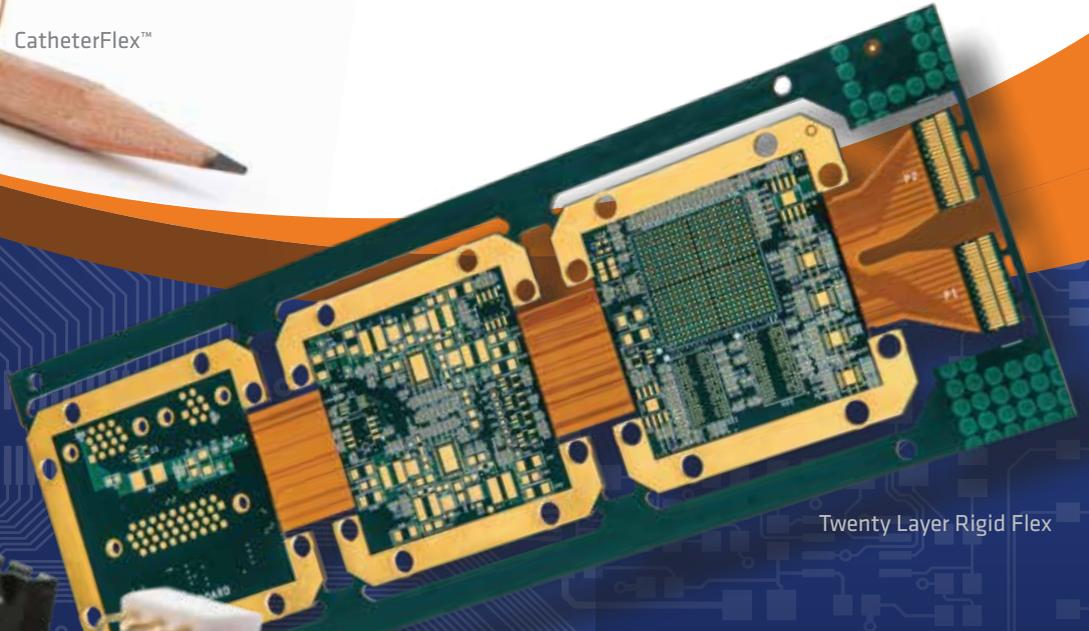
1. Trace fracture

Trace or copper fracture in bend areas. Some examples include presence of trace corners,

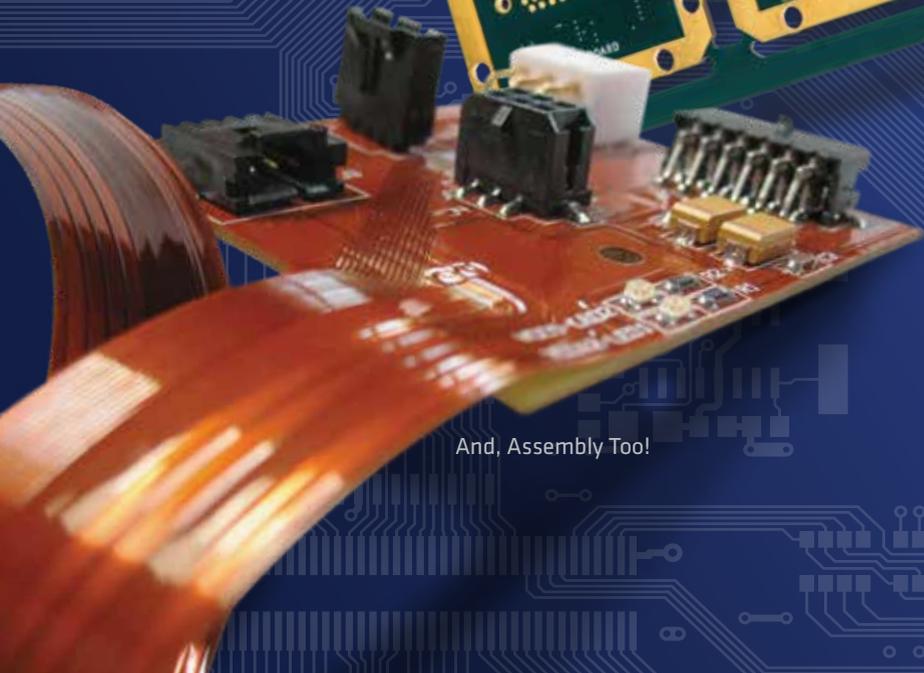
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width transitions, or traces non-perpendicular to the bend axis in a bend area. Also, I-beaming where traces are coincident on adjacent flexible layers.

2. Delamination

Pads or vias in bend areas with improper pad shapes or coverlay exposures. When it is required to have vias or other pads in bend areas, special care must be taken when designing the coverlay to reduce delamination potential. Often in these conditions, the coverlay overlaps the pad area to prevent delamination. In other designs, pads are adorned with tabs to extend under the coverlay.

3. Tearing

The absence of tear stops on slits or inside corners. Copper segments, arcs, circles, or other shapes are added to prevent tear around slits or inside corners.

4. Squeeze out

Epoxy leakage onto adjacent copper or other layer surfaces. In order to prevent epoxy squeeze out, a perimeter air gap or fence must be present around adjacent layer content. For example, a larger annular ring may be required on the epoxy layer than its corresponding coverlay annular ring. This prevents epoxy from squeezing out onto adjacent copper or traces.

5. Button plating

Absence of exposures in coverlay for vias. The most common method of plating vias in a bend area is button plating. This requires vias to be plated have an exposure on their adjacent coverlay. Absence of an exposure on the coverlay would prevent plating.

6. Orphaned conductors

Conductors located outside, or off of, their respective layers. As mentioned previously, absence of individual layer profiles in PCB CAD systems may ultimately lead to orphaned

conductors. Analysis against a board outline rather than a layer's profile is a common cause of this error condition. It puts the onus on a designer to visually inspect layer content for this condition.

7. Coverlay dams

Dams of coverlay between pads rather than ganged exposure. Coverlay is not installed in the same way as liquid photoimageable solder mask. It is a die cut film that does not support thin solder dams between adjacent pads.

8. Layer against layer

Inter-layer dependencies unique to flex and rigid-flex. Many layers in flex and rigid-flex designs are inter-dependent. For example, a RF or shield layer over a conductive layer requires coverlay exposures, contact points between copper, and RF layers to be properly aligned.

9. Area management

The creation and management of stackup zones, bend areas and other regions. Proper analysis requires well defined regions of stackup, bend, flex, rigid and other areas. It is impossible to analyze bend area constraints without precisely defined bend areas.

10. Stackup management

The creation and management of multiple stackups. Almost all rigid-flex designs have multiple stackup areas. To fully analyze a design, the DFM analysis must support the presence of more than one stackup and their related zones of the PCB. Creation and assignment of stackups to zones is required when the data does not provide adequate content for analysis.

11. Intelligent data passing

The ability to pass analyzed data to fabricators in intelligent file formats. After a full DFM analysis, the design should be passed via intelligent file formats to minimize guesswork

at the fabricators. Even a simple intelligent stackup exchange can dramatically improve the process. Gerber remains the standard, but the complexity of rigid-flex designs demands a smarter transfer between designer and fabricator.

Conclusion

Designers and fabricators alike have managed fairly well with limited access to flex-specific DFM analysis tools. Today flex and rigid-flex have become mainstream and the underlying technology is continuously evolving. As is common with all newer technologies, PCB design and analysis tools are playing catch up. PCB CAD tools have now been updated to support design for flex and rigid-flex, but many still lack support needed for intelligent data passing to fabricators. Likewise, most DFM tools have been inadequate to properly analyze flex and rigid-flex designs for manufacturing problems.

We are fortunate to have a long list of users fully enmeshed in flex designs that partnered with us to develop a flex-specific DFM solution. We continue to work with these customers to enhance our capabilities for flex DFM analysis. In addition to the DFM analysis support described in this document, our plans include the ability to analyze additional trace fracture potential such as I-beaming, as well as improved 3D visualization and DFM for a flex and rigid-flex in their bent state. These are just a few examples. Like the underlying technology, the PCB design and analysis tools must also continuously evolve to ensure customer success. **DESIGN007**



Mark Gallant is senior product marketing manager at DownStream Technologies.

Electronics Manufacturers Reporting Cautious Optimism IPC Releases May Global Sentiment of Electronics Supply Chain Report

Per IPC's [May 2023 Global Sentiment of the Electronics Supply Chain Report](#), cost pressures continue to recede and demand remains positive for now, leading to a cautiously optimistic global electronics industry sentiment.

“Geopolitical factors, along with the continued impacts of inflation and rising interest rates, have led manufacturers to describe the current economy as slow, uncertain, challenging, difficult, volatile, and unpredictable,” said Shawn DuBravac, IPC chief economist. “However, despite current conditions, the outlook for 2023 is relatively positive, with manufacturers expressing optimism and expecting growth, especially in the latter half of the year.”

Additional survey results indicate:

- The majority of respondents are still reporting that labor costs and material costs are rising, but the number of companies experiencing rising costs continues to decline. Only 49%

of companies believe material costs will rise in the coming months, the first time this has fallen below 50 percent.

- Ease of recruiting skilled workers has also improved to its highest level since the survey began.
- The Orders Index slipped to 101. This is still in expansionary territory, but it is the lowest level seen since the start of the survey.
- Orders are expected to decline more so for firms operating in North America versus those in Europe, who instead are more likely expecting orders to remain stable.

For the report, IPC surveyed hundreds of companies from around the world, including a wide range of company sizes representing the full electronics manufacturing value chain. [View full report.](#)

The Adjacent Possible

Flexible Thinking

by Joe Fjelstad, VERDANT ELECTRONICS

In the inspirational and informative book titled, *Where Good Ideas Come From*, author Steven Johnson uses the term “the adjacent possible.” This term, which immediately captivated my mind, originated with a theoretical biologist named Stuart Kaufman, who used the term in his book, *Investigations*, to describe the circuitous path of biological evolution. For Johnson, however, the “adjacent possible,” which is one of the places “good ideas come from,” conceptually includes everything that’s one step away from what currently exists, with more is yet to come. This is important. There is a necessary precondition that there must be an immediate nexus to make something “adjacent possible.”

This notion made immediate sense to me as an unrepentant futurist and inventor. I suspect

it is a term that might or should resonate with other inventors as well. One might be able to sense something special waiting to be discovered in the future, but one must first secure their intellectual foothold in the present time and place to successfully take the next step. One must conquer what is near before they can approach and conquer what’s in the distance. Interestingly, once one secures what is adjacent, new adjacencies appear that might cause a beneficial change in thought or direction. In this way, invention is a constant and never-ending process in much the same way that Kaufman envisioned the path of biological evolution in his thesis.

To that end, and with regard to the evolution of the electronics industry, I had an epiphany a few months ago: I realized I had purchased my



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first integrated circuit around 1957 using three months of savings from my paper route. That purchase occurred a full year ahead of Jack Kilby's demonstration of the first integrated circuit which had been cobbled together from a piece of germanium connected to a few resistors and capacitors using gold wires. The integration of transistors for my "integrated circuit" was a very simple printed circuit with six transistors soldered to it. Granted it was a rather large "integrated circuit," but it definitely integrated those transistors and other components and made them work together, allowing me to listen to amplified music from radio stations that were in working proximity.

I cannot say for certain if Kilby had a printed circuit in mind when he built his demonstration, but I know that he worked at CentraLab in Milwaukee, which made ceramic printed circuits for military and commercial customers. Thus, it seems not to be a great stretch of imagination that Kilby saw and took advantage of "the adjacent possible" to create his world-changing invention.

Around the same time—and independently from Kilby—Robert Noyce, then at Fairchild, invented a process for producing defined areas of conductors and insulators on a semiconducting base material, a process that has been continually refined using the concept of "the adjacent possible" ever since, and in the pursuit of extending the life of Moore's law.

Printed circuits also followed the path of the adjacent possible from single metal layer circuits to double-sided boards to multilayer circuits to flex and rigid-flex. So has been the path for assembly from through-hole to surface mount, from one-side assembly to two-side assembly. From the late 1990s to today, the effort has been focused on making circuit features an ever-smaller transition from high-

density interconnections (HDI) to ultra high-density interconnections (UHDI) with feature sizes that are smaller than those used on first-generation integrated circuits.

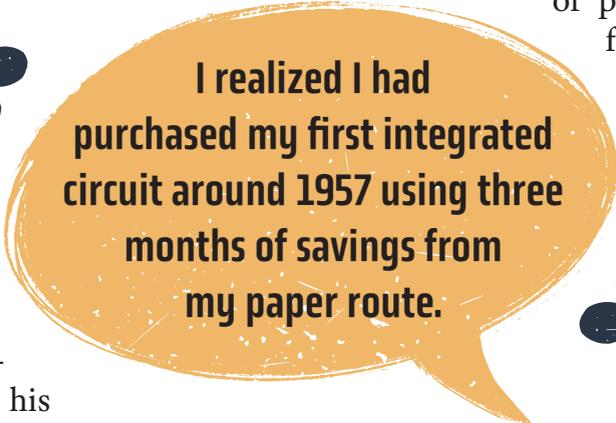
About 15 years ago, the Occam Process was proposed, but it was not considered a step toward the adjacent possible. However, it seems clear that it fits the description. The concept as written up can, by taking a step toward the adjacent possible, potentially address

and solves at one time a number of problems that have long faced the industry. Most of them are related to solder and the problems inherent in the soldering process, especially those related to high temperature damage to circuit board features, such as plated through-holes and electronic components, not to

mention the myriad assembly challenges faced daily by manufacturing engineers.

When viewed in the light of the work of Jack Kilby, the Occam Process, which preaches minimalism in design ("It is vanity to do with more that which can be done with less"—William of Occam), proposes to do something that can be done immediately by simply reversing the process of assembly. That is, rather than building a printed circuit and soldering components to it, build a "component board" and build the circuits required for interconnection for those components on one or both sides of it using processes that are being developed to make HDI and UHDI boards.

These components will ideally have all the same I/O pitch to make board layout easier, as I described several years ago when I suggested in a paper to "dis-integrate" ICs into their constituent IP blocks. Such structures are presently being called "chipselets." It is a step in the right direction but what is largely ignored



I realized I had purchased my first integrated circuit around 1957 using three months of savings from my paper route.

is the need for packages to provide a common pitch and standards for I/O locations providing compatibility between vendors. These ideas have, arguably, always resided in the realm of the adjacent possible and what is next becomes adjacently possible. When the leap is made, the possible begins to expand exponentially, much the way that life has done since it first appeared on this fortunate blue marble in space.

I am inclined to believe that the adjacent possible I see will be embraced in the future, not because time has proven me right many times in the past but because its time is drawing near. As Victor Hugo wrote roughly 150 years ago, “Nothing is more powerful than an idea whose time has come.” I may be dead before that time arrives but the accuracy of my past “innova-

tive predictions” gives me comfort that they will happen once the pain of the status quo becomes unbearable. I must simply follow the guidance of Ted Lasso and “believe.” **DESIGN007**



Joe Fjelstad is founder and CEO of Verdant Electronics and an international authority and innovator in the field of electronic interconnection and packaging technologies with more than 185 patents issued

or pending. To read past columns or contact Fjelstad, [click here](#). Download your free copy of Fjelstad’s book *Flexible Circuit Technology, 4th Edition*, and watch his in-depth workshop series “Flexible Circuit Technology.”

The Journey to IPC-1791 Validation

How does a company protect its most valuable electronics manufacturing information? How can designs and processes be kept safe? IPC-1791 is an industry-driven and industry-written standard that focuses on protecting two things: controlled unclassified information (CUI) and controlled technical information (CTI)—the information that would be devastating for a company to lose.

IPC Validation Services plays a critical role in ensuring that you can keep your information safe. This is the team that performs the Qualified Manufacturer List (QML) audits, validating the manufacturing process to the four pillars: quality, supply chain risk management, security, and chain of custody.

To learn more about how IPC members participate in the process, we spoke with John Vaughan, vice president of strategic markets at Summit Interconnect, who provides insight into his company’s IPC Validation Services journey. If you’re working with defense primes, he says, this certification is vital.

John, please tell us a little about Summit Interconnect.

Summit is the largest privately held printed circuit board manufacturer in North America, featuring eight highly integrated facilities, over one-half million square feet of advanced technology processing capability, and approximately 1,300 employees.

Why did Summit Interconnect decide to certify to IPC-1791?

We operate in very compliance- and certification-driven markets, and we support a heavily DoD and military prime customer set. Our customers have very high expectations in terms of Summit protecting controlled unclassified information (CUI), supply chain risk management (SCRM), chain of custody (CHoC), quality systems (AS 9100), ITAR/EAR, and compliance to NIST 800-171. The IPC-1791 audit and standard is focused on compliance to all these and our position on the IPC-1791 Qualified Manufacturers List (QML) as a Trusted Fabricator gives our customers third-party assurance through the IPC Validation Services that Summit meets specific criteria that are important to them.

To read the rest of this interview, which appeared in the Spring 2023 issue of *IPC Community*, [click here](#).



John Vaughan

Rigid-flex, Rigidized Flex, or Hybrid Flex?

Article by Mike Morando

PFC FLEXIBLE CIRCUITS

In a recent interview with *Design007 Magazine* managing editor Andy Shaughnessy, he asked me about rigid-flex and its new popularity. This seems like a perfect opportunity to dig into the topic and discuss the differentiation between rigid-flex, rigidized flex, and what I am calling a hybrid flex.

The Original: Rigid-flex

Rigid-flex technology was developed years ago for military and aerospace applications. But rigid-flex has become more popular in recent years. Open a cellular phone, for example, and more than likely the internal electronics are mounted on a rigid-flex.

In case you're not familiar with the technology, a rigid-flex is a blend of a rigid printed circuit board and a flex circuit. To manufacture a rigid-flex, a flex circuit is compressed between layers of a rigid PCB design, which leaves the flex area exposed to, well, flex. The rigid areas are, in most cases, used for placing components. The vias/through-holes in both the rigid and flex areas are aligned and plated just like a normal multilayer circuit solution, creating a hybrid, one-piece integrated solution.

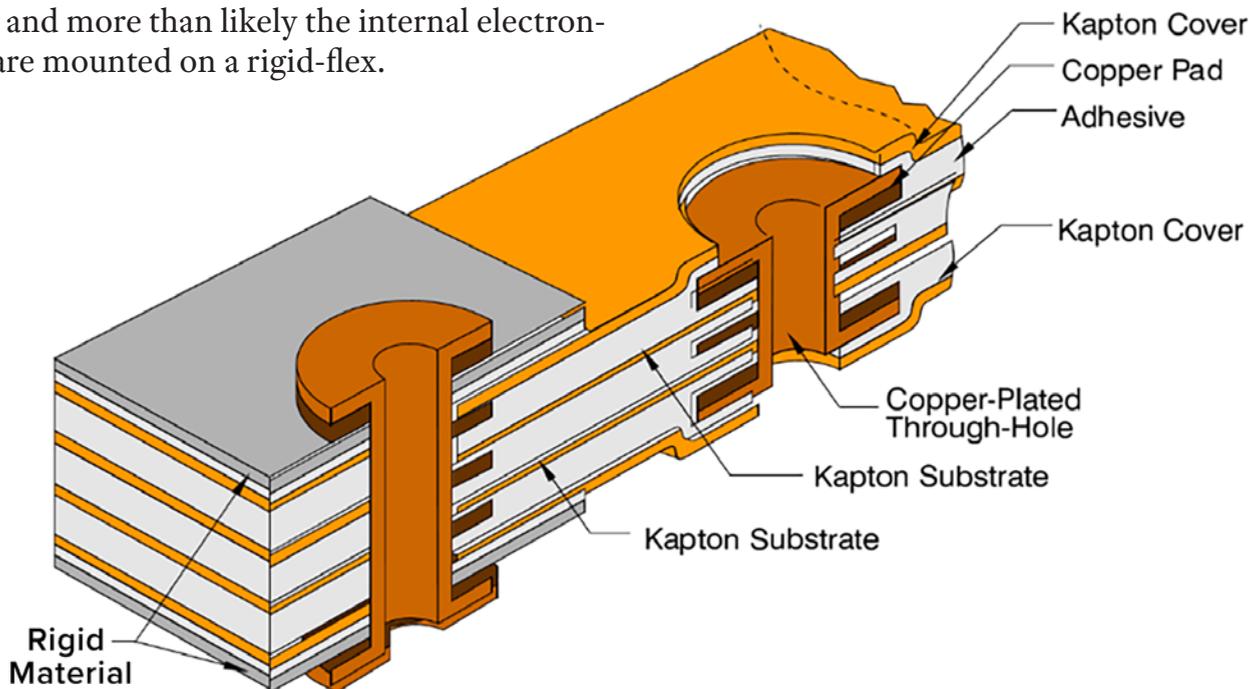


Figure 1: Cross-section of a rigid-flex board.

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BY TAIYO

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- 🏆 High Resolution by photolithography
- 🏆 High Reliability
- 🏆 Simplified process
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- 🏆 Solder mask defined opening (30 μ m diameter)

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Designers of products are learning the advantages of rigid-flex:

- **Denser PCB packaging:** The elimination of interconnect giving the PCB designer more maneuverability and room. PCB real estate has become expensive because there are more components on the boards.
- **Denser system packaging:** This forces designers into 3D solutions. Rigid-flex is the perfect solution because there's more stuff in the package.
- **Simplified assembly:** This means improved reliability, and one-piece installation vs. connectors, cables, and/or additional flex jumpers. This all equals an overall lower cost of manufacturing.
- **Leveraging materials:** The ability to leverage materials from both a PCB and a flex circuit in one integrated package allows for high speed and signal integrity solutions, as well as shielding characteristics.

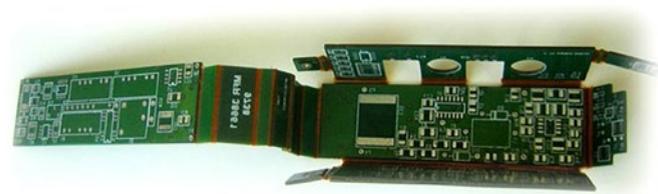


Figure 2.

Possible Disadvantages of Rigid-flex

Rigid-flex is a great solution for the right application. But with good, there is always something else to consider. So, what are the potential “gotchas” with rigid-flex?

- **Cost:** Average rigid-flex cost will be about 20–50% higher than a PCB and 20–30% higher than flex.
- **Volumes:** If there is high volume, the cost curve can flatten. But for North American manufacturing and volumes, the differences in price between a PCB and a rigid-flex can be dramatic.
- **Manufacturability:** Sometimes this is tough. It's based on number of layers and types of materials chosen.

- **Vendor experience:** Does your vendor have experience with rigid-flex and flex?

Rigidized flex: An Alternative Solution

A lower cost alternative to a rigid-flex is a rigidized flex. This is a flex circuit (double-sided or multilayer) that uses a rigid stiffener in place of the PCB portion of the rigid-flex. When you place components on a flex circuit you need to stiffen the area where components will be placed. This stiffened area will assist with SMT placement (prevent flex movement during placement) and prevent solder cracking of the solder joints. We also use stiffeners with through-hole components.

We can use all kinds of materials to create a stiffened area: FR-4, aluminum (heat displacement), machined stainless steel (flatness), ceramic, and additional layers of polyimide.

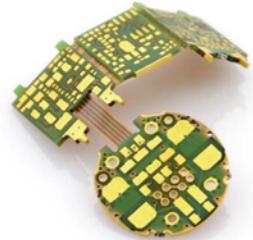
When do we use a rigidized flex?

Honestly, a rigidized flex is common when you need to place components on a flex. However, as a customer considering a rigid-flex, is it possible to put all your components on one side of the flex? If you can, then make a multilayer flex, and add a stiffener. You get all the benefits of a rigid-flex with a lot less cost.



Figure 3: a) Rigidized 3-layer black Kapton with FR-4 stiffener; b) Rigidized 3-layer with FR-4 stiffener.

Focused on Flex



Laser μ Flex series

The versatility and precision of laser processing makes it the ideal tool for machining a wide range of materials.

Typical applications:

- Polymer cover foil
- Covered polymer laminates
- Thin, rigid-flex materials
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- Separation or decap from tracks
- Structuring cavities
- Microvia and through-hole drilling



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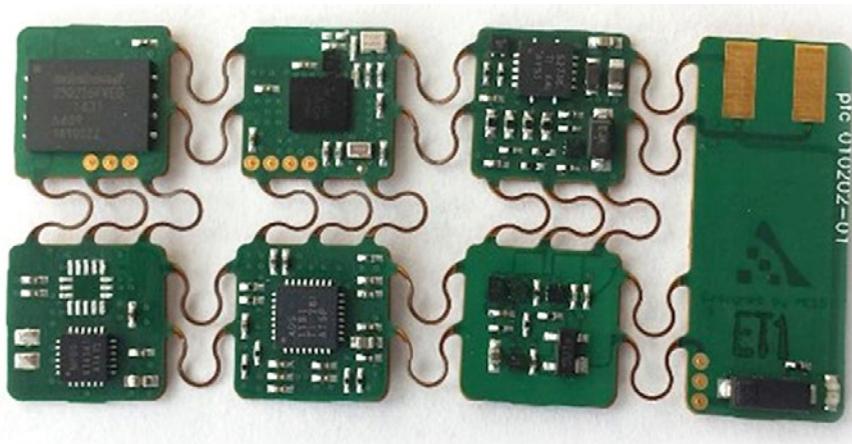


Figure 4: Rigidized 4-layer with FR-4 stiffener.

A Step Further: Hybrid Flex

Let's say you need to have components on both sides. Can you put SMT on one side and through-hole on the other? A simpler version of a rigid-flex can be built as follows: Assume you have a two- to four-layer flex with SMT components on the top or bottom flex side, and through-hole components mounted on the opposite side.

In this instance, instead of building a rigid-flex, one can design the flex and then laminate a simple two-layer rigid board on the bottom. The plated through-holes line up with the plated through-holes in the flex and when the through-hole component is soldered by hand, wave, or a point-to-point soldering system, the solder joins the flex and rigid board together and the through-hole component is securely and electrically anchored in the assembly.

I am calling this a hybrid flex; it's part PCB and part flex. Is there another industry name for this category that I don't know? I'd be happy to hear from you.

The benefits of the hybrid solution are:

- All the benefits of a rigid-flex
- Lower cost



Figure 5: Plated through-holes on the back side of a flex.

They're All Good

Rigid-flex, rigidized flex and hybrid flex are all fantastic solutions. Your manufacturer should be able to steer you based on the flexibility of your design.

If there are so many components required and you need the real estate to place them, forcing you to put them on two sides of the circuit, then a rigid-flex is the right solution for you. It probably has the highest cost and is the most difficult for your supplier to manufacture.

If you can move all the components to one side only, then a rigidized flex is the best solution. It has the lowest cost, and in most cases, is easiest to manufacture.

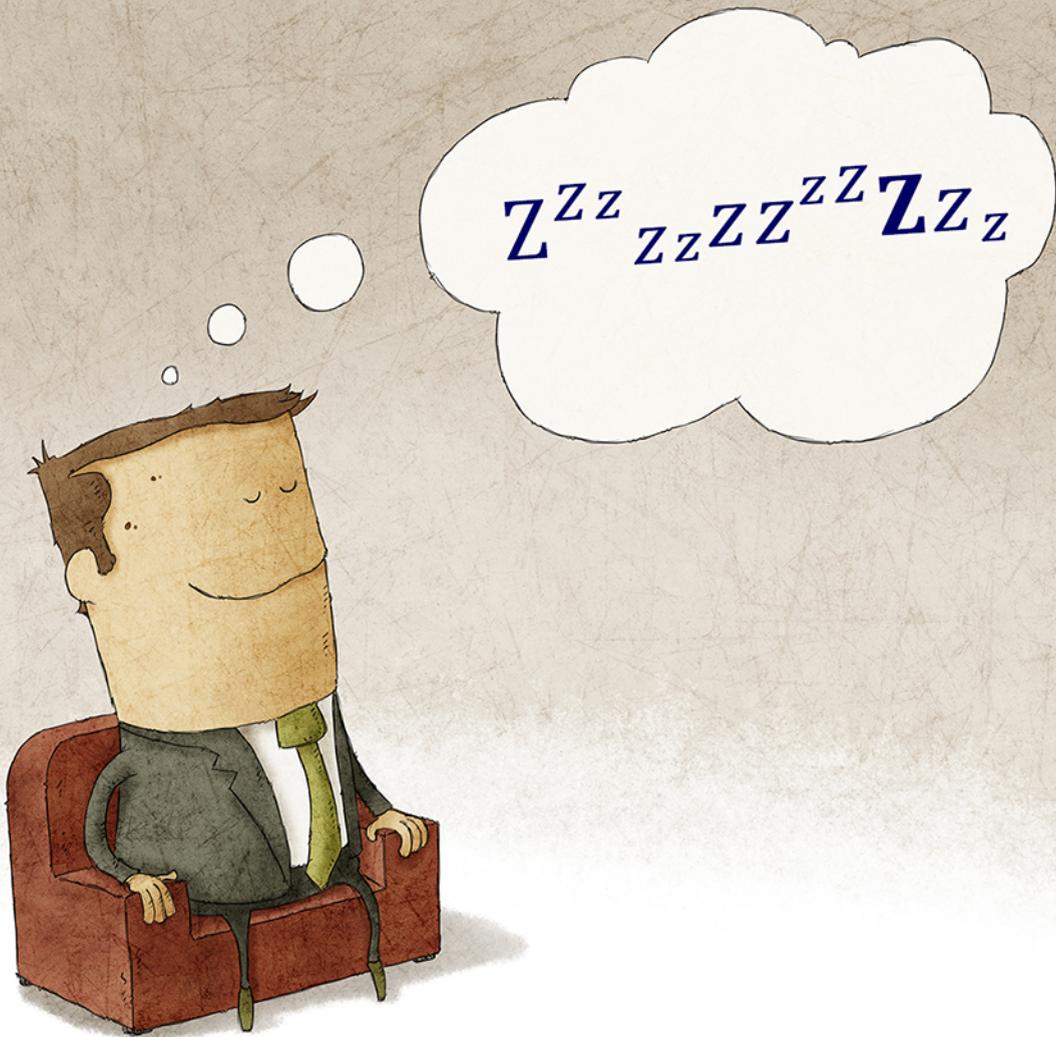
If you have a design that requires components on both sides of a board, SMT on one side, and through-hole on the other, the hybrid solution might be the answer for you.

The bottom line is that the combination of flex circuits and PCBs give designers and manufacturers more maneuverability and, uh, flexibility to package products. **DESIGN007**



Mike Morando is director of sales and marketing for PFC Flexible Circuits, a subsidiary of OSI Electronics.

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– Barry Olney





Slash Sheets and Material Selection

Doug Sober helped pioneer the development of IPC's first slash sheets in 1996 for IPC-4101, Specification for Base Materials for Rigid and Multilayer Printed Boards and we asked him to discuss slash sheets—what they are, what they are not, and why PCB designers might benefit from an IPC materials guide developed specifically for designers.

May 17 Webinar: The Economic Impact of Altium 365

I recently spoke with Fabian Winkler, product marketing manager for Altium 365. He and guest speaker Casey Sirotnak of Forrester co-hosted a free webinar on May 17 titled “Unveil the Total Economic Impact of Altium



365.” Fabian discussed the focus of the webinar and some of the benefits of this environment that allows ECAD and MCAD engineers to collaborate seamlessly.

Stop Over-specifying Your Materials



Columnist Kelly Dack has had a pretty wide range of experiences. As a PCB designer, he has sat behind the desk at an NPI company, an OEM, a fabricator, and now an EMS provider. We asked him to share a few thoughts on the materials selection process and how it could be improved.

Guru & Geezer: A Celebration of the Life of Martin Cotton

The industry lost one of the good ones when Martin Cotton passed away. Martin not only spent 50 years on the cutting edge of PCB design, he was also, as the axiom goes, “a real character.” Everyone who knew Martin has a favorite story about him. He was just a hell of a guy.



Ryan's Hope: From Cop to CAD



I recently ran into Ryan Miller of NCAB Group at SMTA Atlanta. Ryan is a field application engineer and a columnist for Design007 Magazine who joined NCAB last year. In this

interview, Ryan discusses his path from Air Force Security Forces to design engineer, and he outlines what he plans to accomplish at NCAB.

EIPC Review: Ultra-high-density Interconnects, Thin-film Resistor Materials

It's been a little while since I first had the opportunity to review an EIPC Technical Snapshot webinar. The webinar on May 3 was introduced and moderated by EIPC technical director Tarja Rapala-Virtanen. Her first presenter was John Johnson, director of business development at American Standard Circuits, with a detailed case history of ASC's successful realisation of ultra-high-density interconnects.

Altium Announces Launch of Altium 365 GovCloud

Altium has announced the launch of a dedicated region of the Altium 365 cloud platform designed for regulated companies and organizations handling sensitive data. Located on U.S. soil and exclusively managed by U.S. persons in the AWS GovCloud region, Altium 365 GovCloud helps organizations ensure compliance with various U.S. government regulations by choosing an Altium 365 workspace in the GovCloud region.

Select Dielectric Material With Precision

In the past, selecting a dielectric material for PCB fabrication was a no-brainer because we all just used FR-4. Clock frequencies were low and signal rise times were slow, so substrate performance was not an issue. However, in today's multi-gigabit designs, with their extremely fast rise times and tight timing margins, precise material selection is crucial to the performance of the product.



A New Materials Paradigm

As we learned in a recent *Design007 Magazine* survey, when it comes to choosing the right material for their board, our readers are about evenly split. Almost 30% of respondents said they always consult IPC's slash sheets during the



material selection process. One-third said they sometimes use slash sheets in their decision-making progress, but 39% said they never utilize slash sheets.

Dana on Data: Can ChatGPT Solve My PCB Data Transfer Quality Problem?

For decades, humans using software solutions created by humans have been trying to create a perfect PCB design data package that can be utilized, as is, by a PCB fabricator. The goal was to send data to computers that would automatically read and interpret the data and, from that, create production tooling without any human intervention.

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- This position is responsible for expanding our customer network and maintaining existing customer relationships in the Northeast Mexico region. The Sales Engineer would work closely with the German headquarters and the General Manager Rehm Mexico to implement the sales strategy.
- A candidate's proximity to Monterrey, Mexico, is a plus.

Qualifications:

- An engineering degree or comparable qualification with a strong technical background is required.
- Sales-oriented attitude, good communication skills and willingness to travel frequently within Mexico is essential.

We offer innovative products, a great dynamic work environment and exciting training opportunities in our German headquarters.

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Europe Technical Sales Engineer

Taiyo is the world leader in solder mask products and inkjet technology, offering specialty dielectric inks and via filling inks for use with microvia and build-up technologies, as well as thermal-cure and UV-cure solder masks and inkjet and packaging inks.

PRIMARY FUNCTION:

1. To promote, demonstrate, sell, and service Taiyo's products
2. Assist colleagues with quotes for new customers from a technical perspective
3. Serve as primary technical point of contact to customers providing both pre- and post-sales advice
4. Interact regularly with other Taiyo team members, such as: Product design, development, production, purchasing, quality, and senior company managers from Taiyo's group of companies

ESSENTIAL DUTIES:

1. Maintain existing business and pursue new business to meet the sales goals
2. Build strong relationships with existing and new customers
3. Troubleshoot customer problems
4. Provide consultative sales solutions to customers technical issues
5. Write monthly reports
6. Conduct technical audits
7. Conduct product evaluations

QUALIFICATIONS / SKILLS:

1. College degree preferred, with solid knowledge of chemistry
2. Five years' technical sales experience, preferably in the PCB industry
3. Computer knowledge
4. Sales skills
5. Good interpersonal relationship skills
6. Bilingual (German/English) preferred

To apply, email: BobW@Taiyo-america.com with a subject line of "Application for Technical Sales Engineer."

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Career Opportunities



BLACKFOX

Premier Training & Certification

IPC Instructor Longmont, CO

This position is responsible for delivering effective electronics manufacturing training, including IPC certification, to adult students from the electronics manufacturing industry. IPC Instructors primarily train and certify operators, inspectors, engineers, and other trainers to one of six IPC certification programs: IPC-A-600, IPC-A-610, IPC/WHMA-A-620, IPC J-STD-001, IPC 7711/7721, and IPC-6012.

IPC instructors will primarily conduct training at our public training center in Longmont, Colo., or will travel directly to the customer's facility. It is highly preferred that the candidate be willing to travel 25–50% of the time. Several IPC certification courses can be taught remotely and require no travel or in-person training.

Required: A minimum of 5 years' experience in electronics manufacturing and familiarity with IPC standards. Candidates with current IPC CIS or CIT Trainer Specialist certifications are highly preferred.

Salary: Starting at \$30 per hour depending on experience

Benefits:

- 401k and 401k matching
- Dental and Vision Insurance
- Employee Assistance Program
- Flexible Spending Account
- Health Insurance
- Health Savings Account
- Life Insurance
- Paid Time Off

Schedule: Monday thru Friday, 8–5

Experience: Electronics Manufacturing: 5+ years (Required)

License/Certification: IPC Certification—Preferred, Not Required

Willingness to travel: 25% (Required)

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- Solid reputation for on-time delivery (98+% on-time)
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- Production quality quick-turn services in as little as 24 hours
- 5-day standard lead time
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Russ Adams at (206) 351-0281
or russa@prototron.com.

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Career Opportunities



Regional Manager West Region — Two Positions

General Summary: Manages sales of the company's products and services, Electronics and Industrial, within the Pacific Northwest or Southwest Region. Reports directly to Americas Manager. Collaborates with the Americas Manager to ensure consistent, profitable growth in sales revenues through positive planning, deployment and management of sales reps. Identifies objectives, strategies and action plans to improve short- and long-term sales and earnings for all product lines.

DETAILS OF FUNCTION:

- Develops and maintains strategic partner relationships
- Manages and develops sales reps:
 - Reviews progress of sales performance
 - Provides quarterly results assessments of sales reps' performance
 - Works with sales reps to identify and contact decision-makers
 - Setting growth targets for sales reps
 - Educates sales reps by conducting programs/ seminars in the needed areas of knowledge
- Collects customer feedback and market research (products and competitors)
- Coordinates with other company departments to provide superior customer service

QUALIFICATIONS:

- 5-7+ years of related experience in the manufacturing sector or equivalent combination of formal education and experience
- Excellent oral and written communication skills
- Business-to-business sales experience a plus
- Good working knowledge of Microsoft Office Suite and common smart phone apps
- Valid driver's license
- 75-80% regional travel required

To apply, please submit a COVER LETTER and RESUME to: Fernando Rueda, Americas Manager

fernando_rueda@kyzen.com

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Technical Marketing Engineer

EMA Design Automation, a leader in product development solutions, is in search of a detail-oriented individual who can apply their knowledge of electrical design and CAD software to assist marketing in the creation of videos, training materials, blog posts, and more. This Technical Marketing Engineer role is ideal for analytical problem-solvers who enjoy educating and teaching others.

Requirements:

- Bachelor's degree in electrical engineering or related field with a basic understanding of engineering theories and terminology required
- Basic knowledge of schematic design, PCB design, and simulation with experience in OrCAD or Allegro preferred
- Candidates must possess excellent writing skills with an understanding of sentence structure and grammar
- Basic knowledge of video editing and experience using Camtasia or Adobe Premiere Pro is preferred but not required
- Must be able to collaborate well with others and have excellent written and verbal communication skills for this remote position

EMA Design Automation is a small, family-owned company that fosters a flexible, collaborative environment and promotes professional growth.

Send Resumes to: resumes@ema-eda.com

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Career Opportunities



MACHINES FOR PRINTED CIRCUIT BOARDS

Field Service Engineer

Location: West Coast, Midwest

Pluritec North America, Ltd., an innovative leader in drilling, routing, and automated inspection in the printed circuit board industry, is seeking a full-time field service engineer.

This individual will support service for North America in printed circuit board drill/routing and X-ray inspection equipment.

Duties included: Installation, training, maintenance, and repair. Must be able to troubleshoot electrical and mechanical issues in the field as well as calibrate products, perform modifications and retrofits. Diagnose effectively with customer via telephone support. Assist in optimization of machine operations.

A technical degree is preferred, along with strong verbal and written communication skills. Read and interpret schematics, collect data, write technical reports.

Valid driver's license is required, as well as a passport, and major credit card for travel.

Must be able to travel extensively.

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Technical Service & Applications Engineer

Full-Time – Flexible Location

Koh Young Technology, founded in 2002 in Seoul, South Korea, is the world leader in 3D measurement-based inspection technology for electronics manufacturing. Located in Duluth, GA, Koh Young America has been serving its partners since 2010 and is expanding the team with an Applications Engineer to provide helpdesk support by delivering guidance on operation, maintenance, and programming remotely or on-site.

Responsibilities

- Provide support, preventive and corrective maintenance, process audits, and related services
- Train users on proper operation, maintenance, programming, and best practices
- Recommend and oversee operational, process, or other performance improvements
- Effectively troubleshoot and resolve machine, system, and process issues

Skills and Qualifications

- Bachelor's in a technical discipline, relevant Associate's, or equivalent vocational or military training
- Knowledge of electronics manufacturing, robotics, PCB assembly, and/or AI; 2-4 years of experience
- SPI/AOI programming, operation, and maintenance experience preferred
- 75% domestic and international travel (valid U.S. or Canadian passport, required)
- Able to work effectively and independently with minimal supervision
- Able to readily understand and interpret detailed documents, drawings, and specifications

Benefits

- Health/Dental/Vision/Life Insurance with no employee premium (including dependent coverage)
- 401K retirement plan
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Arlon EMD, located in Rancho Cucamonga, California, is currently interviewing candidates for open positions in:

- Engineering
- Quality
- Various Manufacturing

All interested candidates should contact Arlon's HR department at 909-987-9533 or email resumes to careers.ranch@arlonemd.com.

Arlon is a major manufacturer of specialty high-performance laminate and prepreg materials for use in a wide variety of printed circuit board applications. Arlon specializes in thermoset resin technology, including polyimide, high Tg multifunctional epoxy, and low loss thermoset laminate and prepreg systems. These resin systems are available on a variety of substrates, including woven glass and non-woven aramid. Typical applications for these materials include advanced commercial and military electronics such as avionics, semiconductor testing, heat sink bonding, High Density Interconnect (HDI) and microvia PCBs (i.e., in mobile communication products).

Our facility employs state of the art production equipment engineered to provide cost-effective and flexible manufacturing capacity, allowing us to respond quickly to customer requirements while meeting the most stringent quality and tolerance demands. Our manufacturing site is ISO 9001: 2015 registered, and through rigorous quality control practices and commitment to continual improvement, we are dedicated to meeting and exceeding our customers' requirements.

For additional information, please visit our website at www.arlonemd.com

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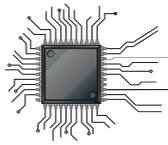
Are You Our Next Superstar?!

Insulectro, the largest national distributor of printed circuit board materials, is looking to add superstars to our dynamic technical and sales teams. We are always looking for good talent to enhance our service level to our customers and drive our purpose to enable our customers to build better boards faster. Our nationwide network provides many opportunities for a rewarding career within our company.

We are looking for talent with solid background in the PCB or PE industry and proven sales experience with a drive and attitude that match our company culture. This is a great opportunity to join an industry leader in the PCB and PE world and work with a terrific team driven to be vital in the design and manufacture of future circuits.

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Career Opportunities



MivaTek

Global

Field Service Technician

MivaTek Global is focused on providing a quality customer service experience to our current and future customers in the printed circuit board and microelectronic industries. We are looking for bright and talented people who share that mindset and are energized by hard work who are looking to be part of our continued growth.

Do you enjoy diagnosing machines and processes to determine how to solve our customers' challenges? Your 5 years working with direct imaging machinery, capital equipment, or PCBs will be leveraged as you support our customers in the field and from your home office. Each day is different; you may be:

- Installing a direct imaging machine
- Diagnosing customer issues from both your home office and customer site
- Upgrading a used machine
- Performing preventive maintenance
- Providing virtual and on-site training
- Updating documentation

Do you have 3 years' experience working with direct imaging or capital equipment? Enjoy travel? Want to make a difference to our customers? Send your resume to N.Hogan@MivaTek.Global for consideration.

More About Us

MivaTek Global is a distributor of Miva Technologies' imaging systems. We currently have 55 installations in the Americas and have machine installations in China, Singapore, Korea, and India.

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Qualifications and skills

- A love of teaching and enthusiasm to help others learn
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- Soldering and/or electronics/cable assembly experience
- IPC certification a plus, but will certify the right candidate

Benefits

- Ability to operate from home. No required in-office schedule
- Flexible schedule. Control your own schedule
- IRA retirement matching contributions after one year of service
- Training and certifications provided and maintained by EPTAC

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Career Opportunities



American Standard Circuits

Creative Innovations In Flex, Digital & Microwave Circuits

CAD/CAM Engineer

Summary of Functions

The CAD/CAM engineer is responsible for reviewing customer supplied data and drawings, performing design rule checks and creating manufacturing data, programs, and tools required for the manufacture of PCB.

Essential Duties and Responsibilities

- Import customer data into various CAM systems.
- Perform design rule checks and edit data to comply with manufacturing guidelines.
- Create array configurations, route, and test programs, panelization and output data for production use.
- Work with process engineers to evaluate and provide strategy for advanced processing as needed.
- Itemize and correspond to design issues with customers.
- Other duties as assigned.

Organizational Relationship

Reports to the engineering manager. Coordinates activities with all departments, especially manufacturing.

Qualifications

- A college degree or 5 years' experience is required.
- Good communication skills and the ability to work well with people is essential.
- Printed circuit board manufacturing knowledge.
- Experience using CAM tooling software, Orbotech GenFlex®.

Physical Demands

Ability to communicate verbally with management and coworkers is crucial. Regular use of the telephone and e-mail for communication is essential. Sitting for extended periods is common. Hearing and vision within normal ranges is helpful for normal conversations, to receive ordinary information and to prepare documents.

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APCT

Passion | Commitment | Trust

APCT, Printed Circuit Board Solutions: Opportunities Await

APCT, a leading manufacturer of printed circuit boards, has experienced rapid growth over the past year and has multiple opportunities for highly skilled individuals looking to join a progressive and growing company. APCT is always eager to speak with professionals who understand the value of hard work, quality craftsmanship, and being part of a culture that not only serves the customer but one another.

APCT currently has opportunities in Santa Clara, CA; Orange County, CA; Anaheim, CA; Wallingford, CT; and Austin, TX. Positions available range from manufacturing to quality control, sales, and finance.

We invite you to read about APCT at APCT.com and encourage you to understand our core values of passion, commitment, and trust. If you can embrace these principles and what they entail, then you may be a great match to join our team! Peruse the opportunities by clicking the link below.

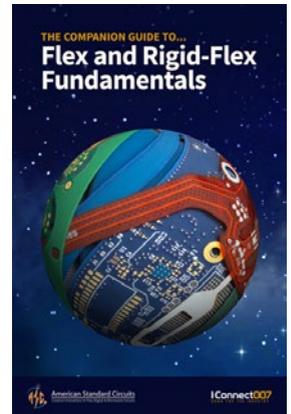
Thank you, and we look forward to hearing from you soon.

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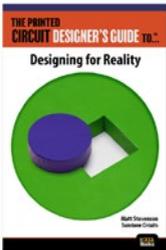
NEW!

THE COMPANION GUIDE TO... FLEX AND RIGID FLEX FUNDAMENTALS

I-Connect007 and American Standard Circuits are proud to announce the launch of the companion guide to the immensely popular *The Printed Circuit Designer's Guide to... Flex and Rigid-flex Fundamentals*. This short guide, written by topic experts at American Standard Circuits, is designed to provide additional insights and best practices for those who design or utilize flexible and/or rigid-flex circuit boards. Topics covered include trace routing options, guidelines for process optimization, dynamic flexing applications, rigid-to-flex transition and more. Visit I-007ebooks.com to download your copy.



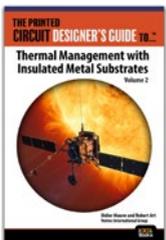
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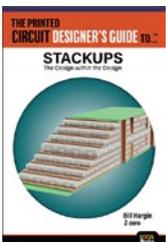
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